The Impact of Radiation Effects on Satellite Electronics

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Course Outline

- ❖ **Motivation: Why Managing Radiation Response is Critical**
- ❖ **Basic Device Overview and Generalized SAT Systems**
- ❖ **Primer: Space Environment**
- ❖ **Basic Radiation Effects Mechanisms**
- ❖ **Practical Real-World Examples of Radiation Effects**
- ❖ **General Guidance for Building Space Systems**
- ❖ **Total Ionizing Dose: Lab Notes**

Motivation: Space Mission Success

Image from https://www.teslarati.com/spacex-next-starlink-launch-worlds-largest-constellation/

From Associated Press (Feb. 10, 2022)

"CAPE CANAVERAL, Fla. (AP) — SpaceX's newest fleet of satellites is <u>tumbling out of orbit after being struck by a solar storm"</u>

40 of 49 satellites either reentered the atmosphere and burned up, or are on the verge of doing so…

SpaceX said…*geomagnetic storm…made atmosphere denser, which increased the drag on the Starlink satellites, effectively dooming them…*

BUT ACTUALLY, satellites **<u>failed to awaken</u>** and could not be told to climb to a higher, more stable orbit, according to the company.

Did radiation-induced events cause "failure to awaken" event in 80% of SpaceX satellites?

Basic Device Overview and Generalized SAT Systems

Space Application Systems / Components

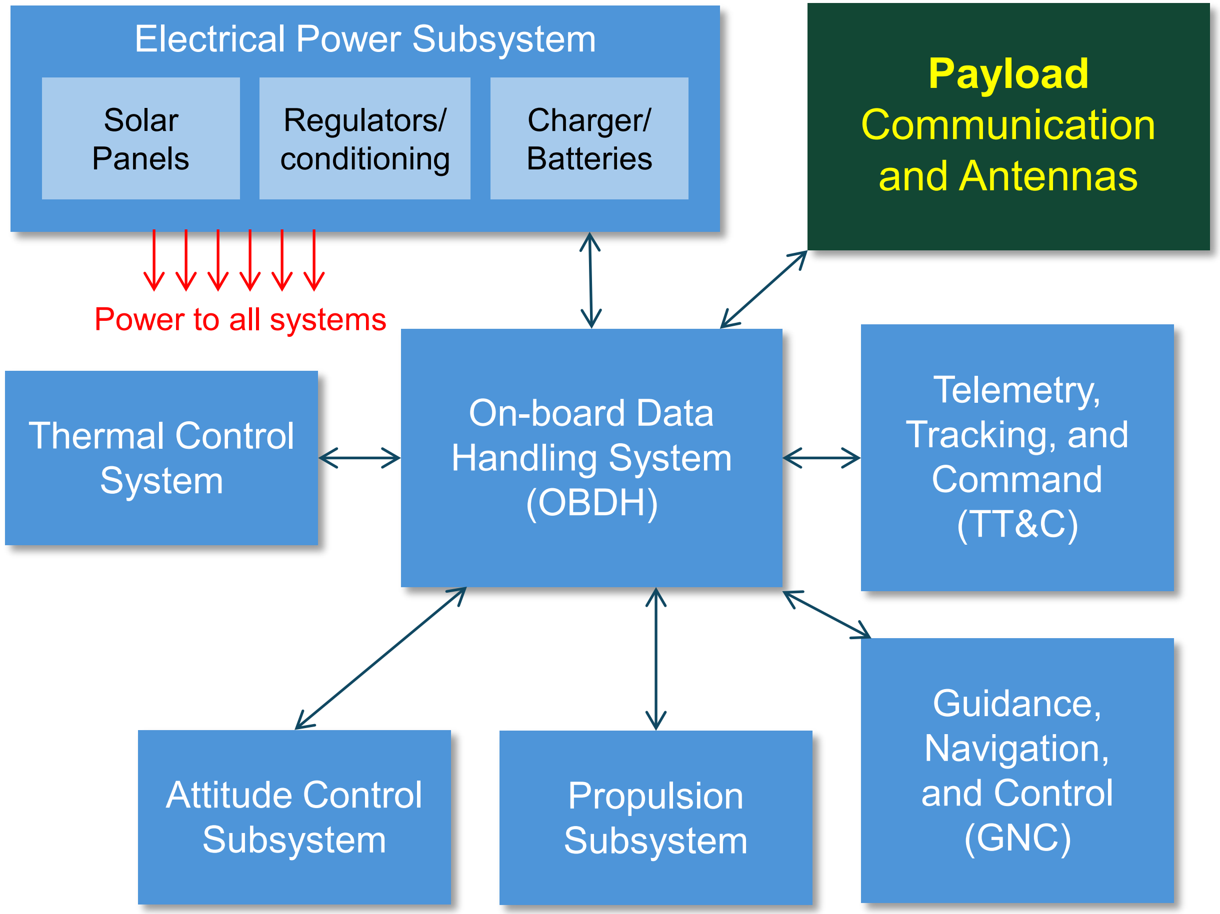
Analog Domain — **Digital Domain**

SIMPLE → ***COMPLEX***

Discretes/Simple ICs

Power systems
Diodes/MOSFETs/Bipolars
Load switches
Low drop out (linear regulators) regulators
Boost-Buck converters
Voltage references
Temp, I, V sensors

Signal/Sensor Chain
Analog switches
Amplifiers, Buffers
Comparators



ICs to SoCs

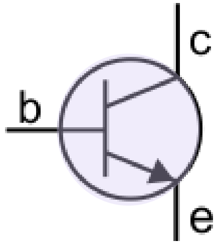
Digital Operations
Clocks/Conditioners
Digital switches/MUXes
Control logic
Line buffers/Line conditioners
Level translators
ADC/DAC
Rf Signal Processing
CMOS/CCD Image sensors

Controllers
Interface controllers
Ethernet/Gigabit controllers
COM chips
NVRAM and SDRAM
MCUs, CPUs, DSPs

Transistors as “Charge Faucets”

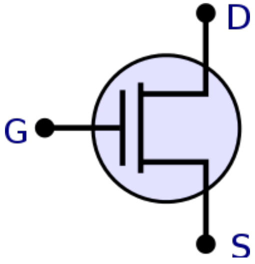
Control

Control

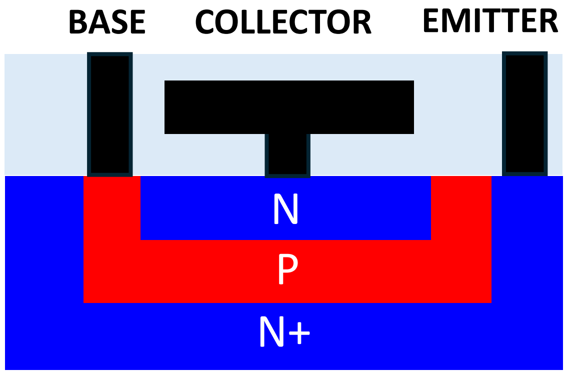


Both use MOS structure!!

Control



Bipolar Junction Transistor (BJT)



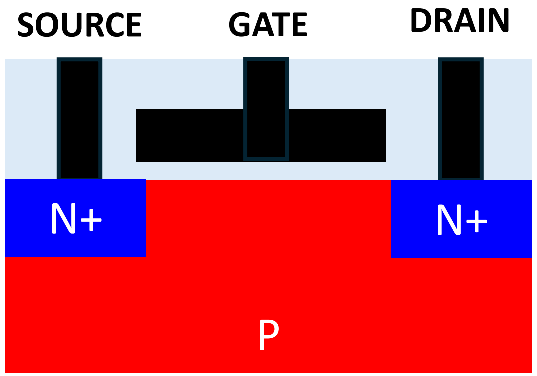
Current controlled “faucet”

Small BASE current controls level of larger current (Collector to Emitter)

Minority and Majority Carrier Device

Analog electronics & power

Field-Effect Transistor (FET)



Voltage controlled “faucet”

Small GATE VOLTAGE controls state of much larger voltage (Drain to Source)

Majority Carrier Device

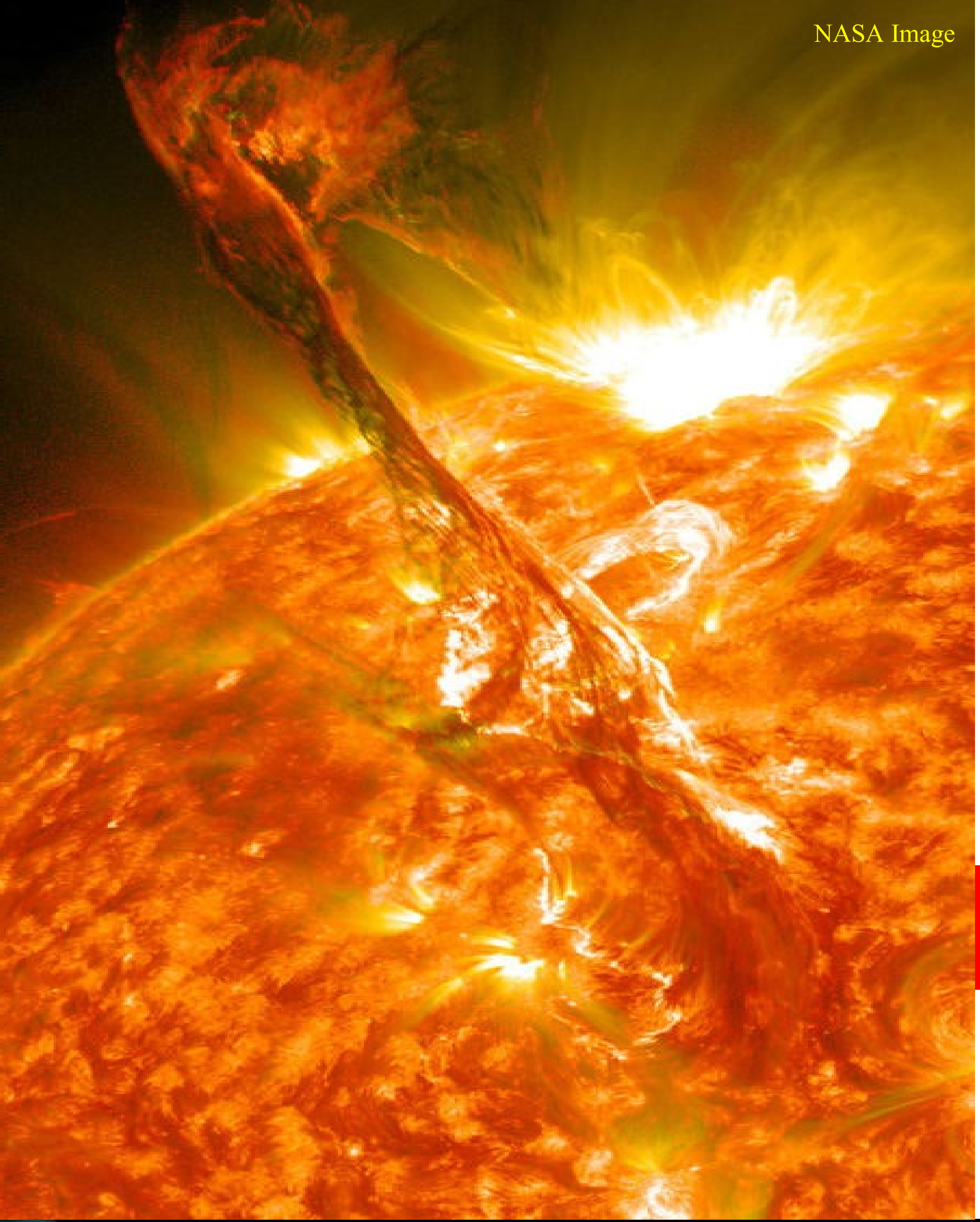
Control, digital switching & computation

Primer: Space Environment

Orbital Altitude Nomenclature

- Low Earth Orbit (**LEO**): 500 - 2,000 km [R_{earth} = 6,370 km]
- Medium Earth Orbit (**MEO**): 2,000 km – 35,786 km
- Global Positioning System (**GPS**): 20,513 km (orbit every 12 hours)
- GEO stationary (**GEO**) orbit / Geosynchronous Orbit (**GSO**): 35,786 km (orbit every 24 hours)
- High Earth Orbit (**HEO**): > 35,786 km (transfer orbits)
- Sun Synchronous Orbit (SSO): Polar orbit (various altitudes)

https://www.youtube.com/watch?v=z4H3kR-9fM0



Space is a Harsh Mistress

Mechanical
- Vibration / Shock / Acceleration
- Vacuum / Pressure changes
- Stress cycling (thermally induced)
- Impact (orbital debris)

Chemical
- Outgassing (vacuum) / Moisture – Plastic vs. Ceramic
- Metal bond robustness (Cu, Au, vs. Al)
- TIN whiskers in solder alloys

Large temperature ranges (-55° to 125°C) or more?

Magnetic fields, EMI/EMC, electrical charging effects

Atomic Oxygen/Erosion of satellite surfaces

High Radiation Environment => **TID, DDD, SEE** in Electronics & Materials

Quality & Reliability in ICs and Passives
- Time-zero Quality & Early Failures

Atmospheric Drag (LEO/MEO)/Solar Radiation Pressure

Location, Location, Location!!!

Location	Primary Radiation Sources	Shielding Factors	Approximate Dose Rate	Dominant Reliability Concerns
Earth Surface	Secondary neutrons, muons, terrestrial primordial isotopes (40K, U, Th), Radon	Maximum: Deep magnetosphere + thick atmosphere + 2π sr planet shielding	~0.001 mSv/day (~0.3–0.4 mSv/year)	Single-Event Effects (SEEs) from neutrons (e.g., terrestrial SEUs, multi-bit upsets in dense SRAMs/DRAMs)
LEO / MEO (e.g., ISS)	Trapped protons/electrons (SAA), GCRs, attenuated SPEs	Heavy geomagnetic shielding, solid planet blocks 2π sr	~0.5 to 1 mSv/day	SEUs, SETs, low-to-moderate TID
GEO	Trapped outer-belt electrons, unshielded GCRs & SPEs	None (outside effective shielding)	~1 to 5 mSv/day (highly variable)	High TID/TNID, Deep Dielectric Charging, heavy ion SEEs
Lunar Surface	Unshielded GCRs, severe SPEs, secondary albedo neutrons	Solid moon blocks 2π steradians; no magnetosphere or atmosphere	~2 to 3 mSv/day (background GCR)	Extreme SPE spikes, GCR-induced SEEs, albedo neutron displacement damage
Martian Surface	Attenuated GCRs and SPEs, atmospheric secondary neutrons	Thin atmosphere (20 g/cm2), solid planet blocks 2π sr	~0.6 to 0.7 mSv/day	Secondary neutron-induced SEEs, long-term cumulative TID
Io Surface (moon of Jupiter)	Ultra-energetic trapped relativistic electrons and ions	Extreme Jovian magnetosphere interaction	~360,000 mSv/day (36 Sv/day)	Catastrophic TID failure within hours, severe DD, extreme SEE rates, SEL/SEGR

Max "safe" dose
0.0027 mSv/d

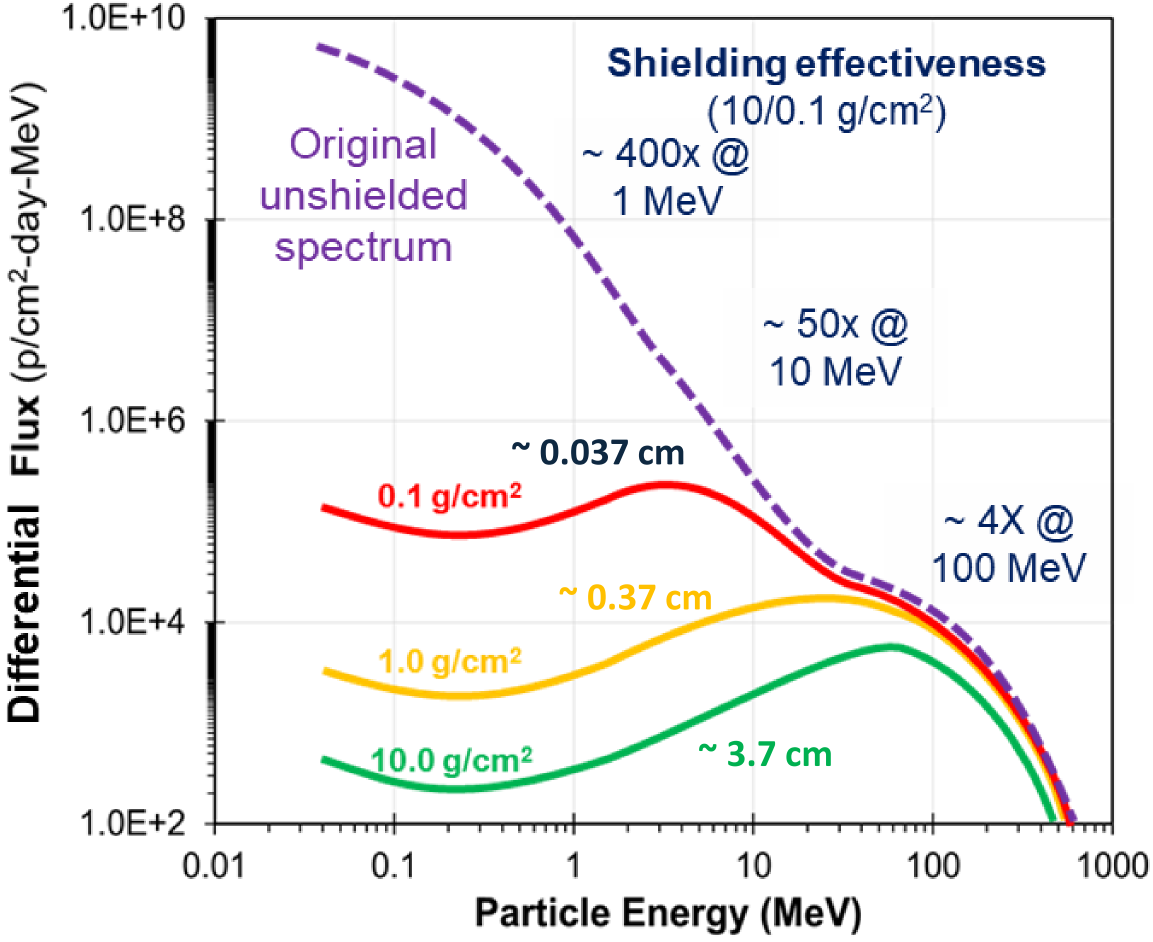
Non Lethal, "Radiation sickness" dose
1 Sv

"Fatal" dose
10 Sv

The **Sievert (Sv)** is the International System of Units (SI) used to measure the health risk of ionizing radiation on the human body. **Unlike purely physical measurements of radiation DOSE, the Sievert is a biological dose unit quantifying the actual biological damage that radiation poses to living tissue.**

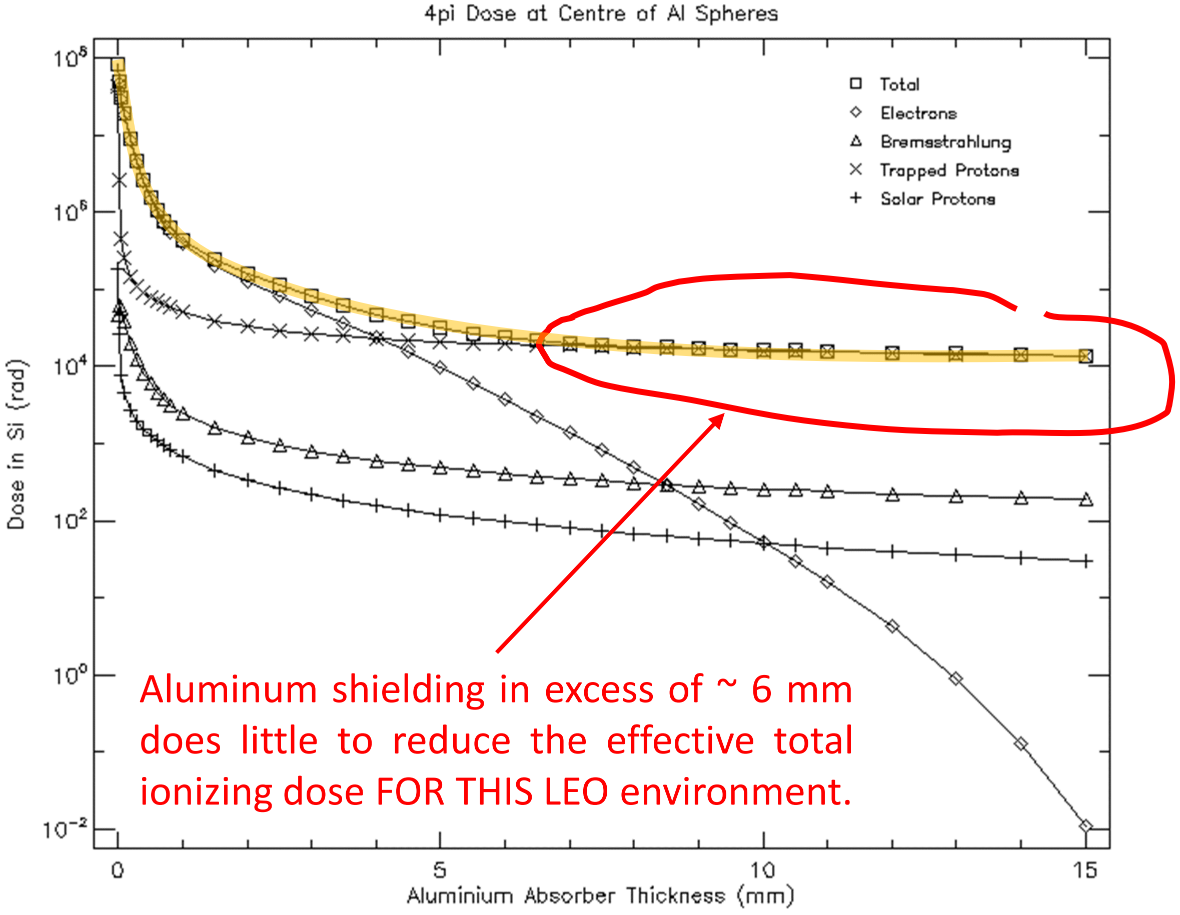
Can't we just shield the electronics???

Proton SEE vs. Shielding Thickness



Adapted from E. Stassinopoulos and J. Raymond, "The Space Radiation Environment for Electronics," Proc. IEEE, Vol. 76, p. 1423, 1988.

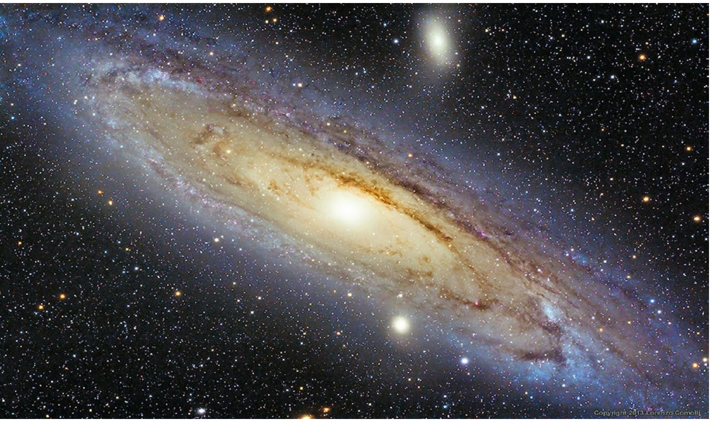
TID vs. Shielding Thickness



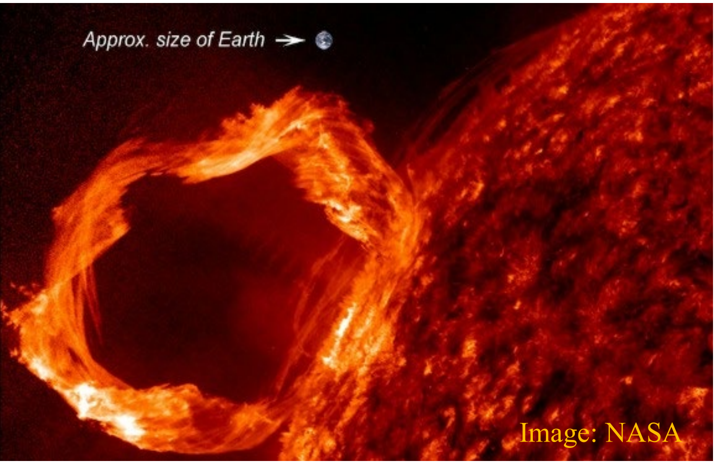
Dose depth curves for aluminum shielding for solar min conditions, LEO, 500km altitude, and 60 degree inclination. Calculated with SPENVIS.

Space Radiation Environment

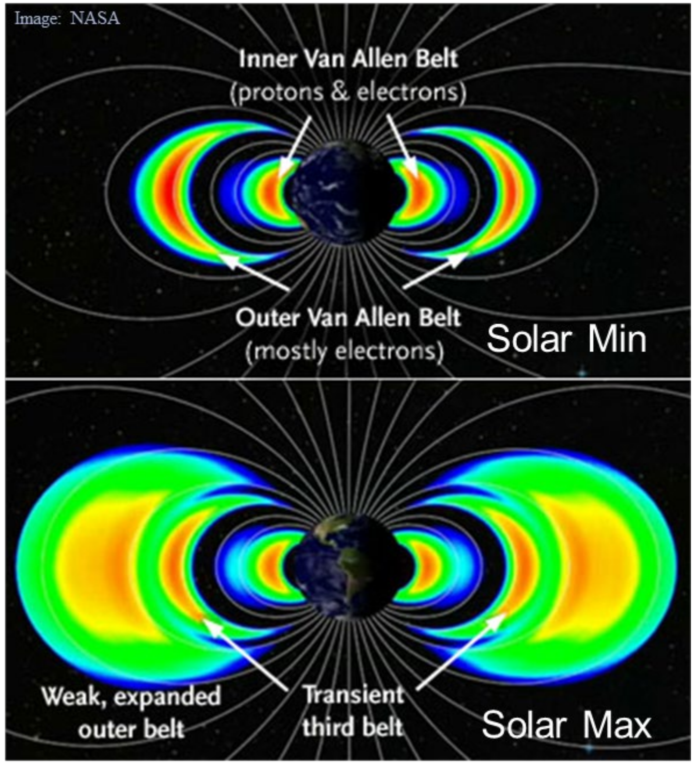
INPUT SOURCES → **TRANSFER FUNCTION (Shielding & Trapping)** → **OUTPUT: ION FLUX vs. LET**



Galactic Cosmic Rays (GCRs)



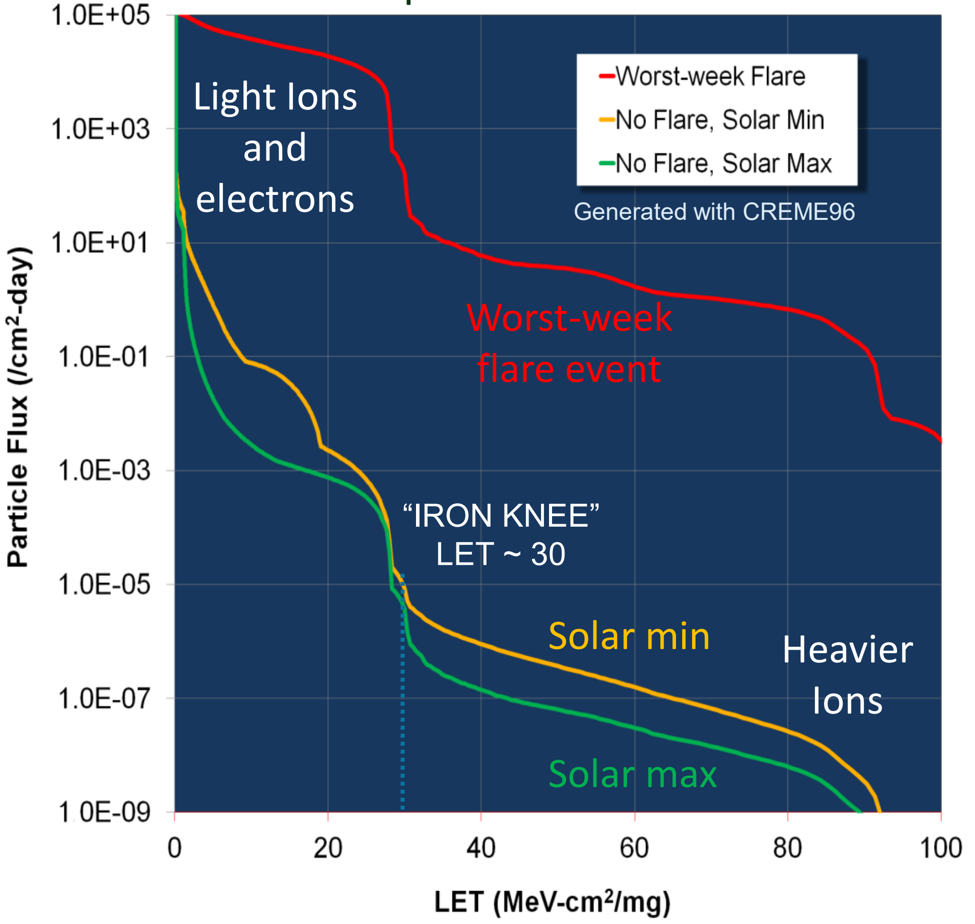
Solar Energetic Particles (SEPs)



Trapped particles + shielding

Specific Orbital Parameters
(apogee, perigee, inclination, solar cycle, shielding)

Flux spectrum for LEO orbit

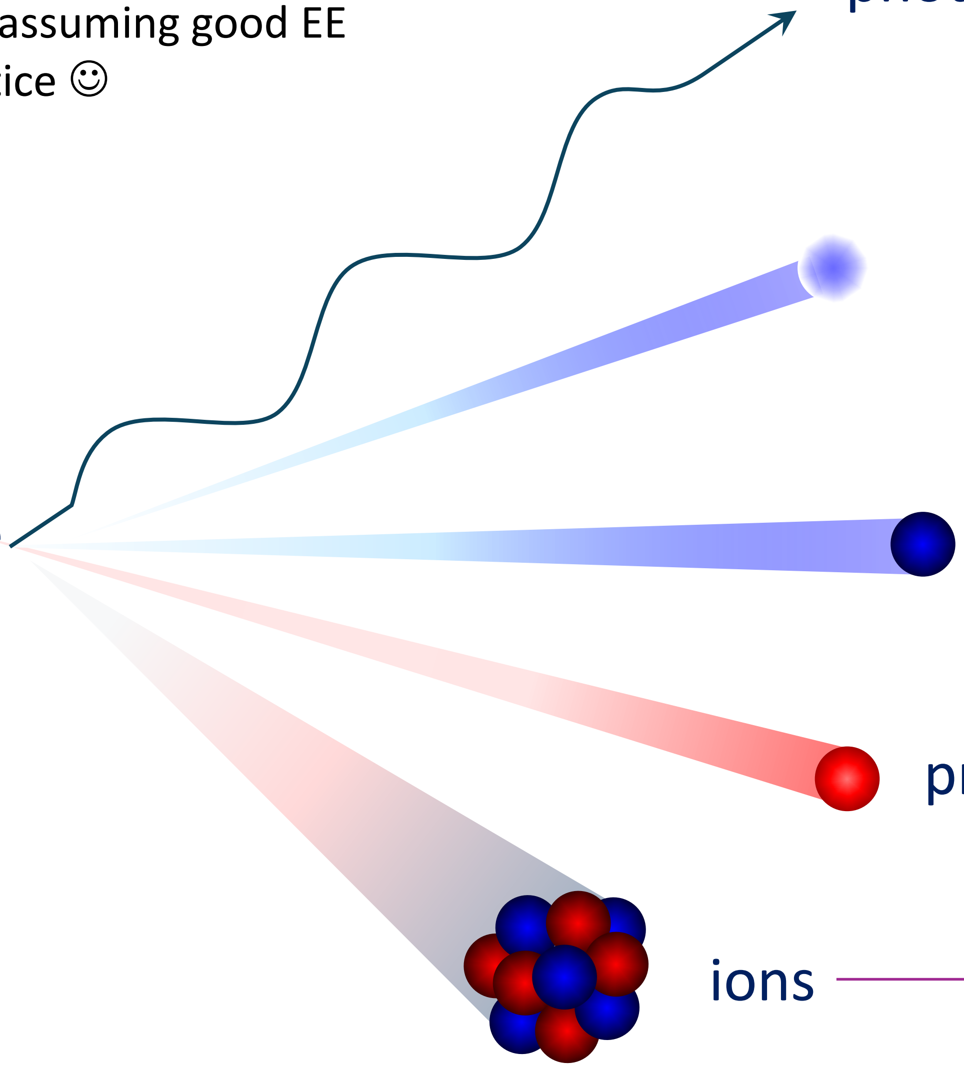


Lots of protons (solar, GCR, trapped), electrons (trapped), and much more rare heavier ions

Basic Radiation Effects Mechanisms

What Is Particle Radiation?

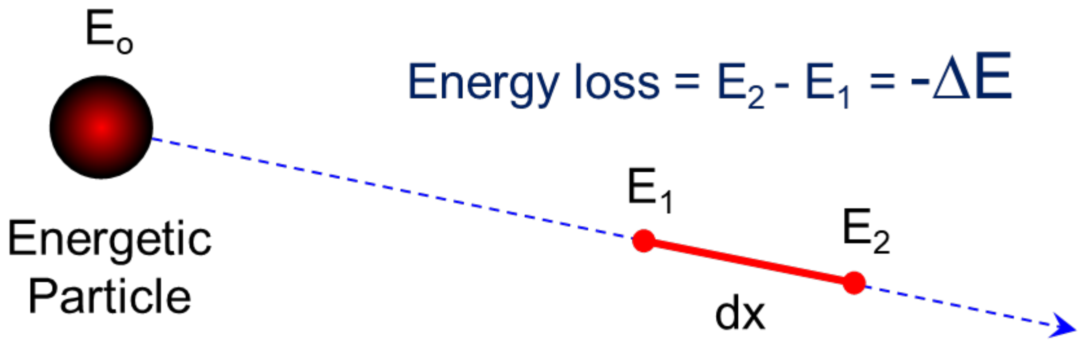
We do not consider EMI/EMC as a contributor assuming good EE design practice ☺



Source

- photons → Space: TID (Brems. gammas)
- Electrons → Space: TID
- neutrons → Terrestrial: SEE (moon, etc.)
- protons → Space: TID, DD, SEE
- ions → Space: SEE

Ion Strength: Linear Energy Transfer (LET)



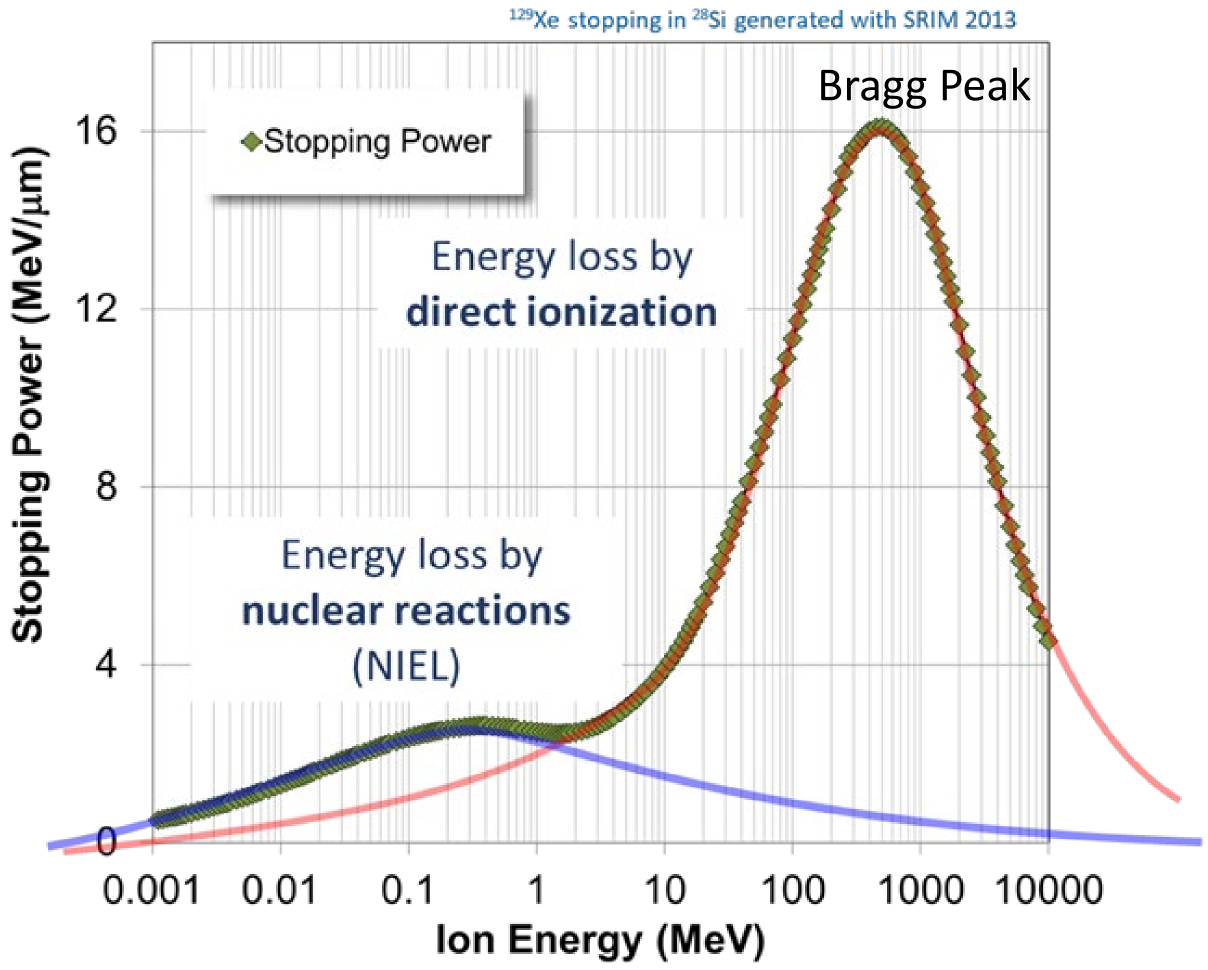
Energy loss = $E_2 - E_1 = -\Delta E$

$LET = (dE/dx)_{elec}$

Stopping power (LET) is determined by ion type (Z) its kinetic energy AND the target material. LET is the amount of energy absorbed by material per unit length travelled by the ion!

LET is **non-linear** = at lower energies (when the ion is moving more slowly) the stopping power reaches a maximum (Bragg peak)

Range is inversely proportional to the LET. The higher the LET the shorter the range. Higher energy particles have greater range.

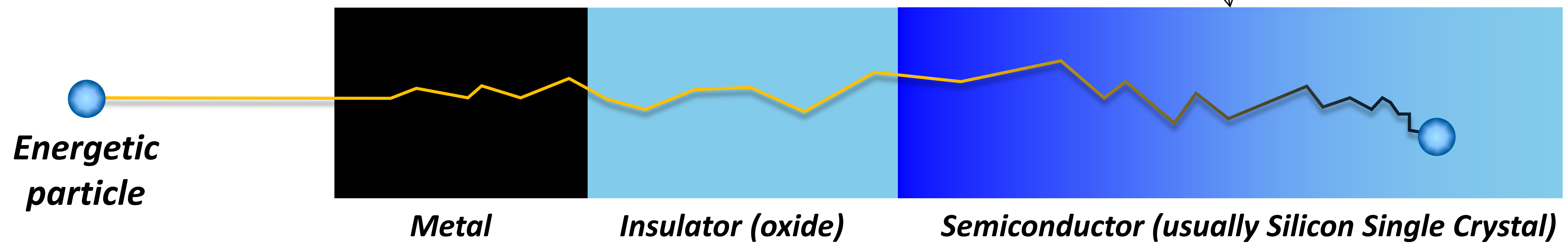


Radiation absorbed loses most of its energy by producing charge in materials, only a small fraction is related to nuclear reactions/atomic damage.

Material Interactions and Effects in MOS

Charge generated by radiation event in metal small compared to free charge => **minimal impact**. Metals are amorphous or poly-crystalline so atomic-level structural damage has little effect => **minimal impact.**

Transient charge generated by event is large compared to free charge. Dissipated by recombination, drift, and diffusion. Resultant **charge transient => big impact**. Particle also can cause structural damage that affects electrical/optical properties of single crystals **=> big impact**.



Charge generated in oxide is very large compared to free charge. **Charge transported and trapped => big impact**. Most oxides amorphous so **structural damage has minimal impact**.

"MOS Stack" is used to form both FET and BJT devices

3 Key Radiation Effects

- **Transient charge generation in semiconductors**
- **Charge trapping in insulators**
- **Displacement damage**

Total Non-Ionizing DOSE (TNID, DD)

Total Ionizing DOSE (TID)

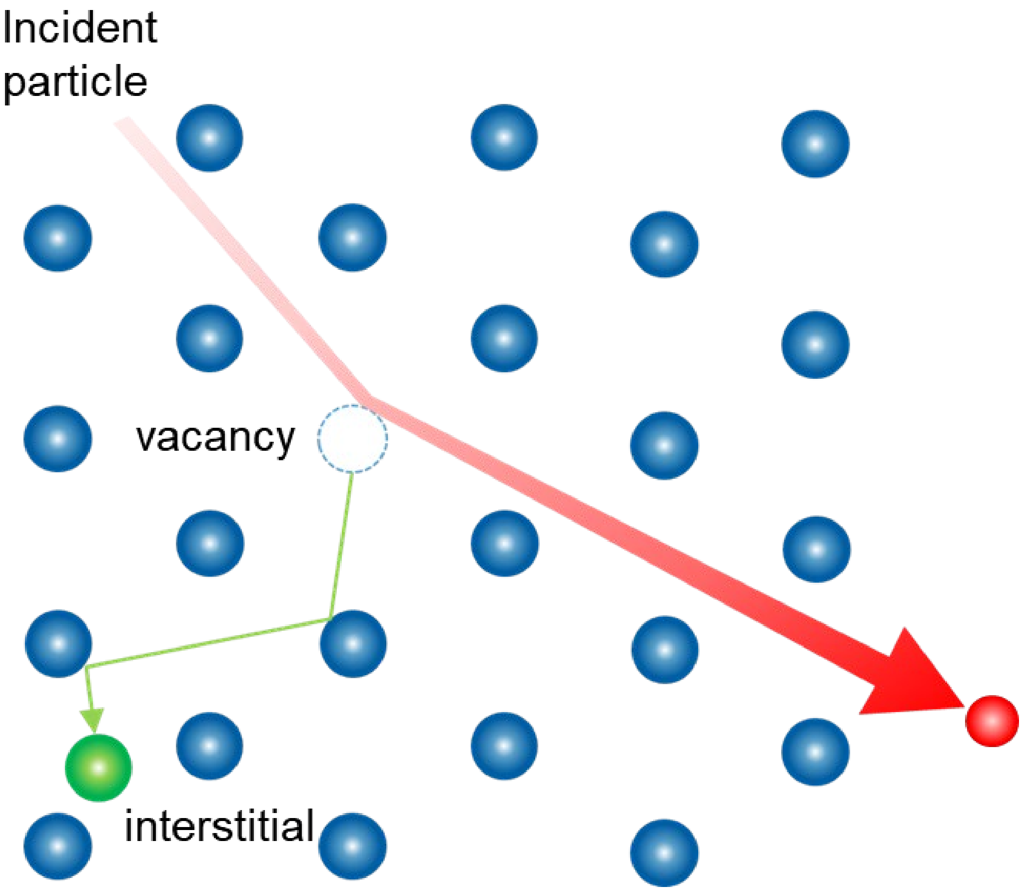
Single Event Effects (SEEs)

Total NON-Ionizing Dose (TNID, DD)

- Accumulated exposure to many events over mission time (chronic exposure). **Like a sunburn (it takes billions of “events” to cause sunburn)!**
- Absorbed energy creates **atomic defects (displacement damage)** in the **VOLUME of the material**.
- In highly ordered single-crystal substrates the accumulation of defects has a profound impact on the electronic properties (created mid-band traps that greatly increase carrier recombination/generation).
- Damage is independent of applied voltage! Happens even if IC is off!!!
- Effects: β reduction in BJTs as base minority carrier lifetime is reduced. To a lesser degree, I_D reduction in MOS due to reduced majority carriers in channel (usually at least 1000x LESS sensitive so BJTs fail long before FETs).
- **Aging at the atomic level!**

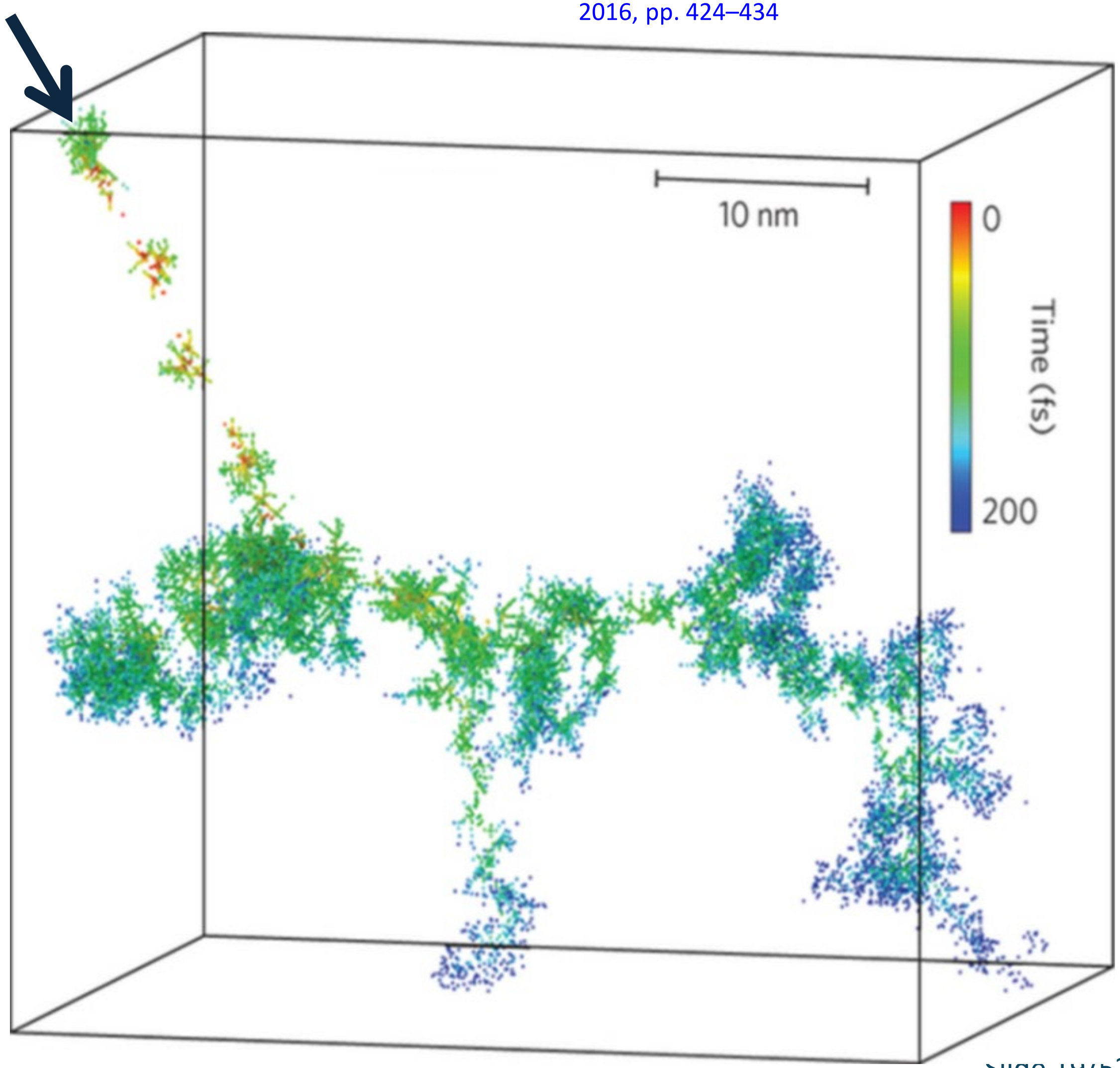
Mick Jagger after chronic dose exposure (…to sex, drugs, and rock & roll)!

Displacement Damage



Incident 200MeV Neutron-induced recoil (in Iron)

J. Knaster, A. Moeslang, and T. Muroga, "Materials research for fusion," *Nature Physics 12*, May 2016, pp. 424–434

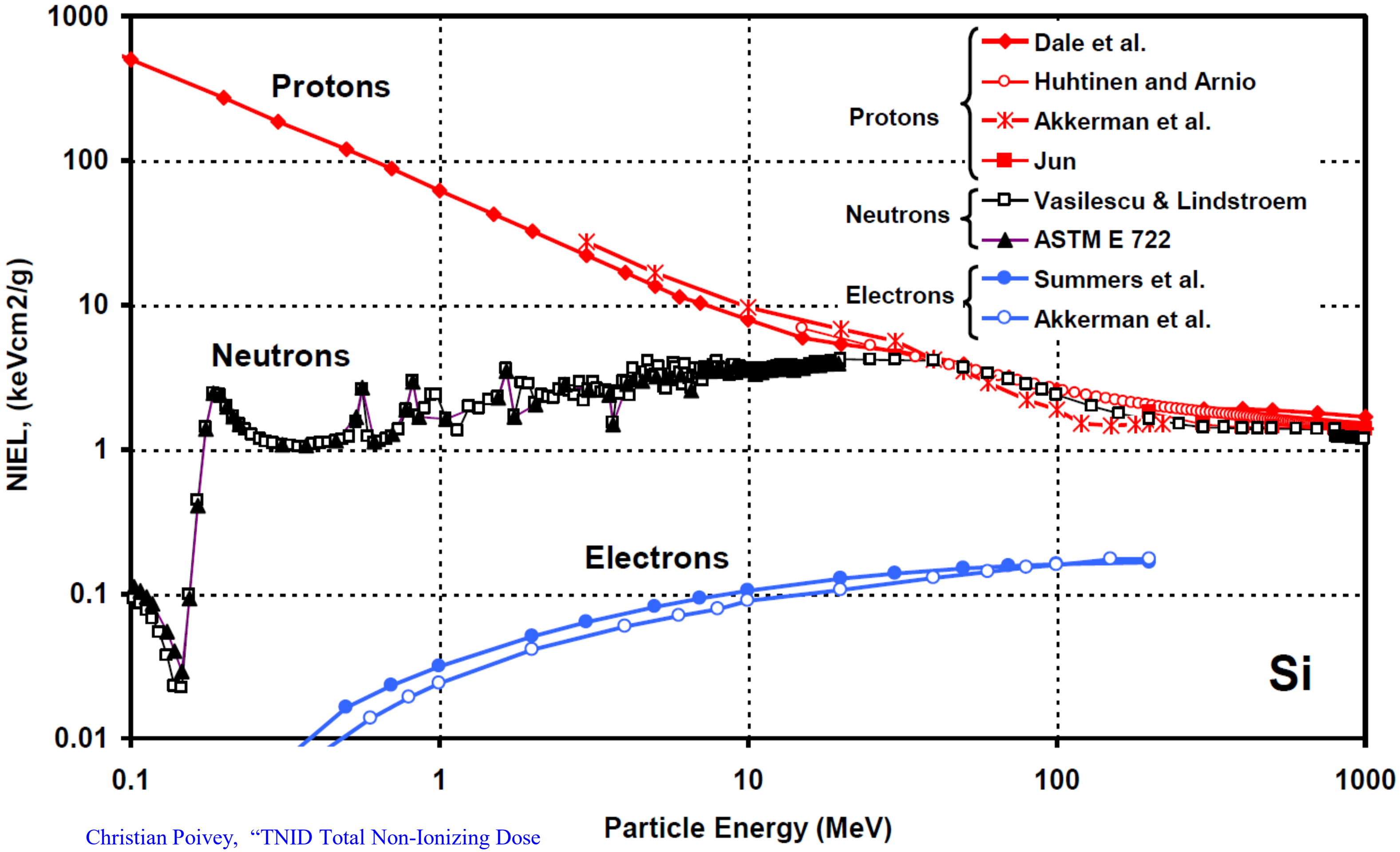


Incident particles SOMETIMES cause target atoms to be removed from their lattice sites producing vacancies and interstitials (**displacement damage**).

While some of these defects "anneal out" with interstitials recombining with vacancies, a small % of them will combine as bound "Frenkel pairs" (a separated vacancy and interstitial pair) **becoming electrically active**.

Damage depends on particle energy and type

NIEL = Non-Ionizing Energy Loss ~ displacement damage



Christian Poivey, "TNID Total Non-Ionizing Dose or DD Displacement Damage," ESA CERN SCC Workshop, May 9 10, 2017

Protons create the most NIEL because they possess higher mass and charge. Protons make up most of space radiation hence DD is maximized in space (LEO orbits in the Van Allen belts are worst-case since there are huge densities of trapped protons).

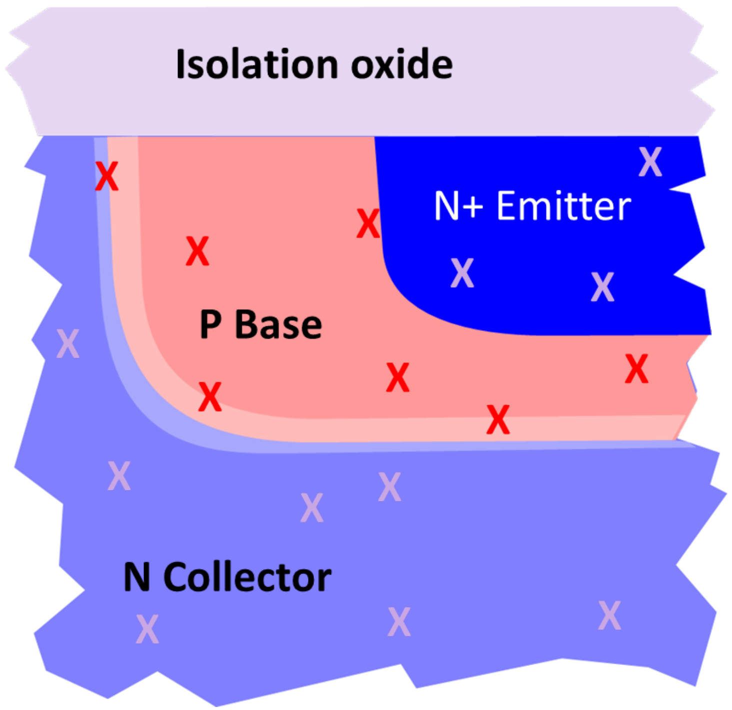
Neutrons do NOT have a direct Coulomb scattering interaction so, at low energy, neutron NIEL is much lower than that of protons. Since their mass is almost the same as protons above 40 MeV both nucleons create similar levels of damage where coulomb interactions are not dominant.

Electrons are much less massive than the proton or neutron (~ 1/2000) and thus create far less NIEL.

Heavier ions with higher charges will potentially create even more NIEL than protons but these are rare even in space so displacement damage from heavier ions is usually not significant.

DD is worst-case for lower energy protons

Impact of Displacement Damage on BJT



Defects in the base volume (X) dominate the degradation

Majority carrier devices (MOSFETs) can usually sustain much higher levels of displacement damage.

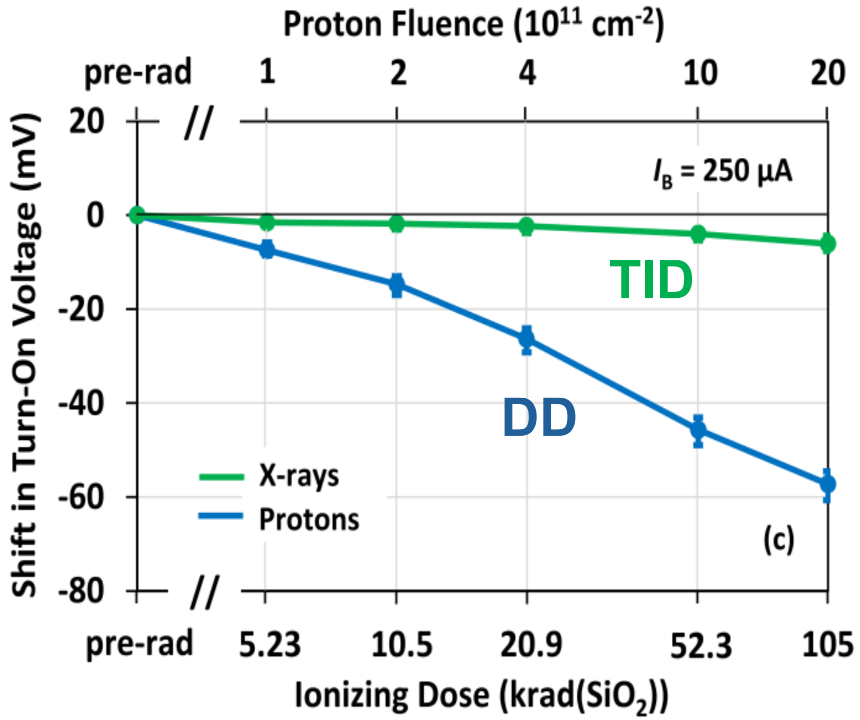
↑ $I_B \sim \uparrow R_{bulk(base)} + R_{surface(base)}$

As defects in the base region increase, recombination in base increases, requiring more base current to be injected into the base to create the same collector current

$$\downarrow \beta = \frac{I_C}{I_B \uparrow}$$

Current gain (β) goes down (I_B increases) as damage dose increases

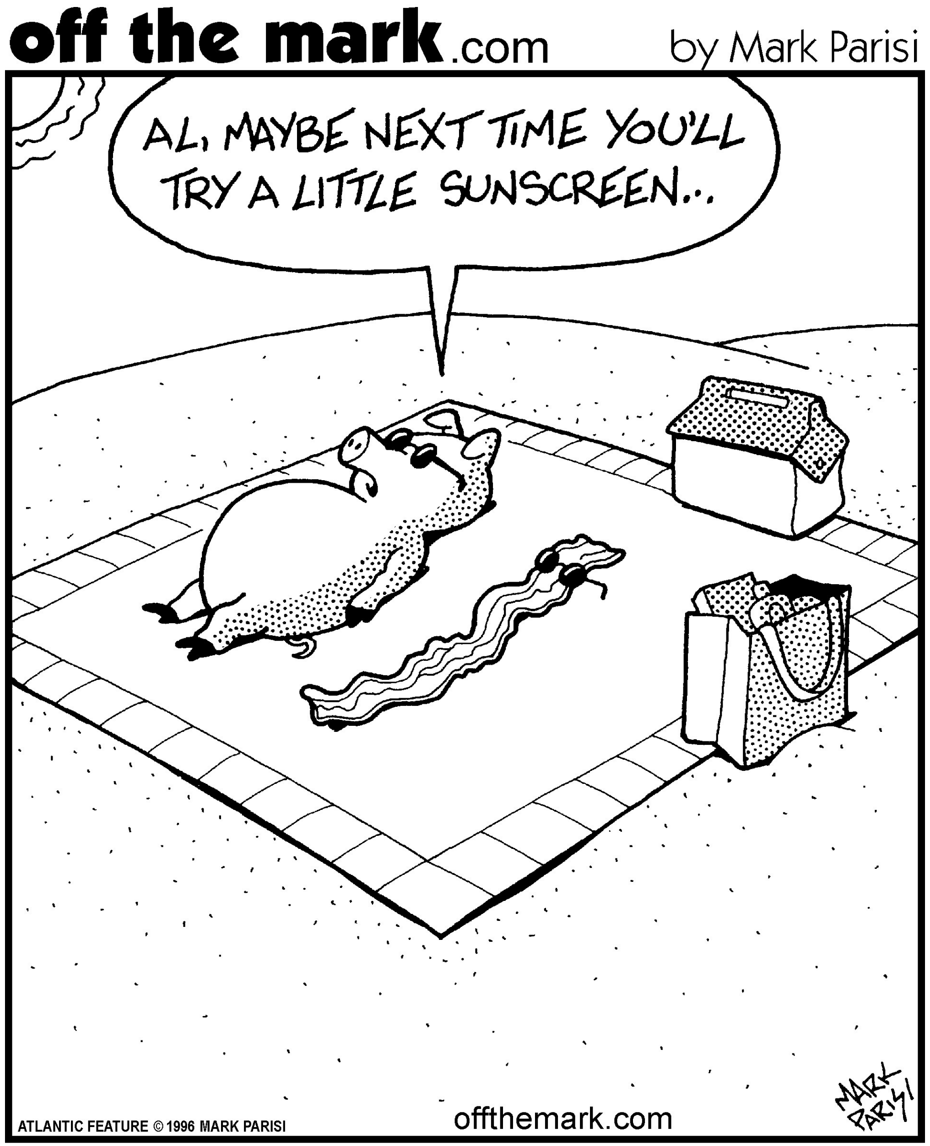
2N5339 NPN Bipolar Transistor



Steven C. Witczak et al, "Damage Separation in a Bipolar Junction Transistor Following Irradiation With 250-MeV Protons," IEEE Trans. Nucl. Sci., VOL. 66(5), MAY 2019

Gamma rays only produce TID while protons produce a smaller amount of TID and lots of DD – since the shift in turn-on is greater with protons this implies the part is dominated by DD sensitivity.

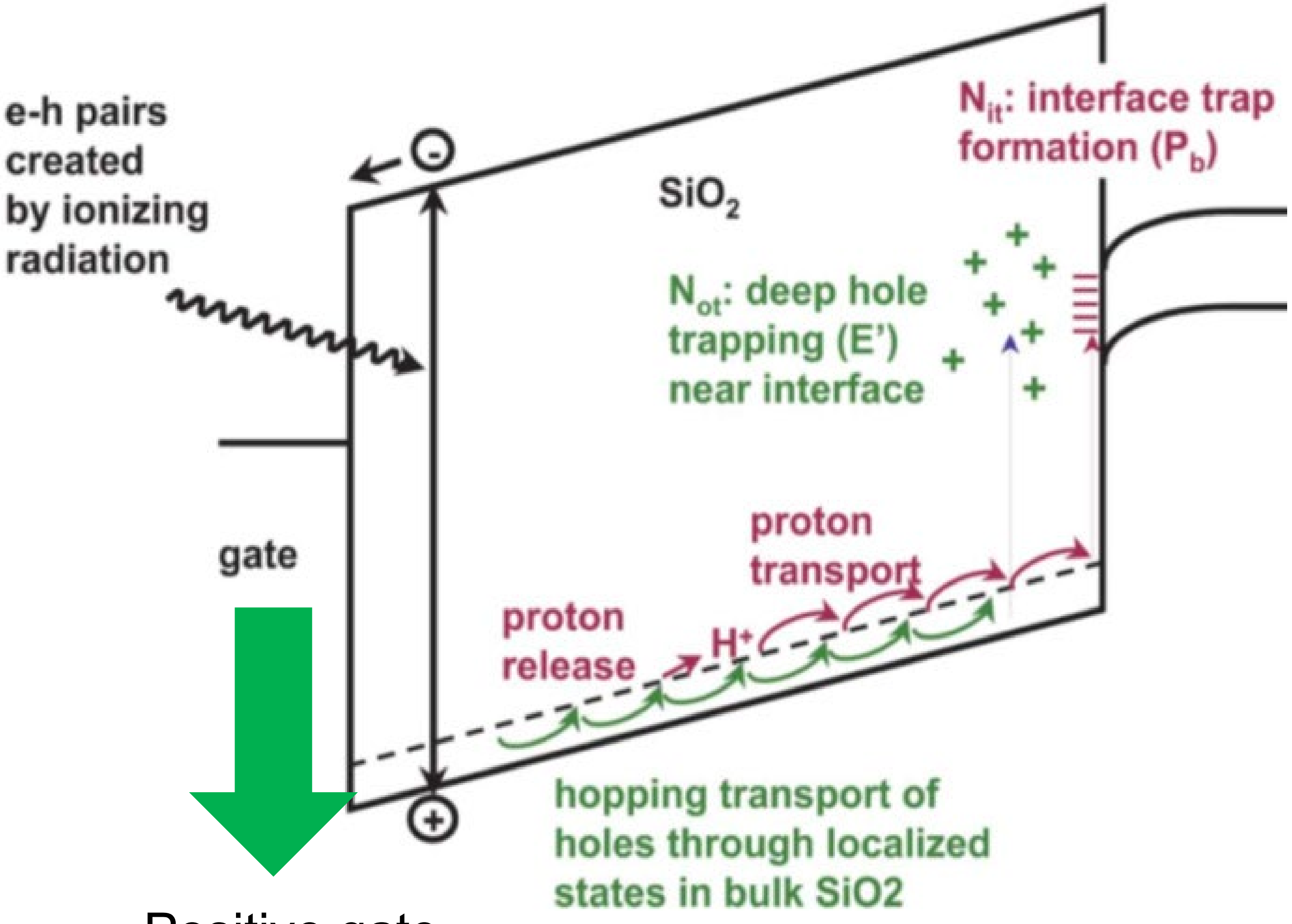
Total Ionizing Dose (TID)



Permission for Texas Instruments to use cartoon in print/electronic.

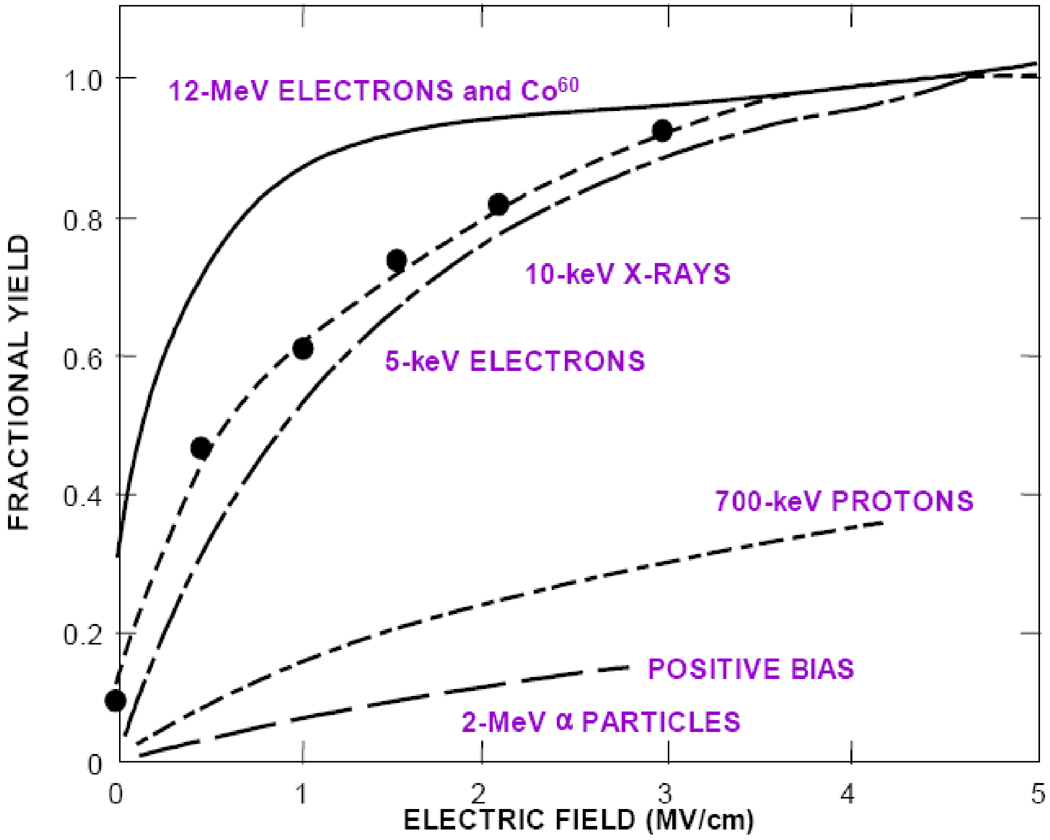
- Accumulated exposure to many radiation events (chronic).
- Absorbed energy creates charge in oxide VOLUME.
- Electrons are free to leave, leaving trapped hole charge.
- Holes move to the interface by drift and diffusion.
- Charge trapped near, and defect states created at the Si:SiO_2 interface induce quasi-permanent device shifts.
- V_{TH} shifts in MOSFETs, gain reduction in BJTs.
- Effect is volumetric, a larger oxide volume = larger effect.
- Since charge transport is involved, applied field makes a big difference in the TID effect (bias is usually worse than no bias) HOWEVER TID damage can still occur with NO BIAS!

Basic TID Mechanism



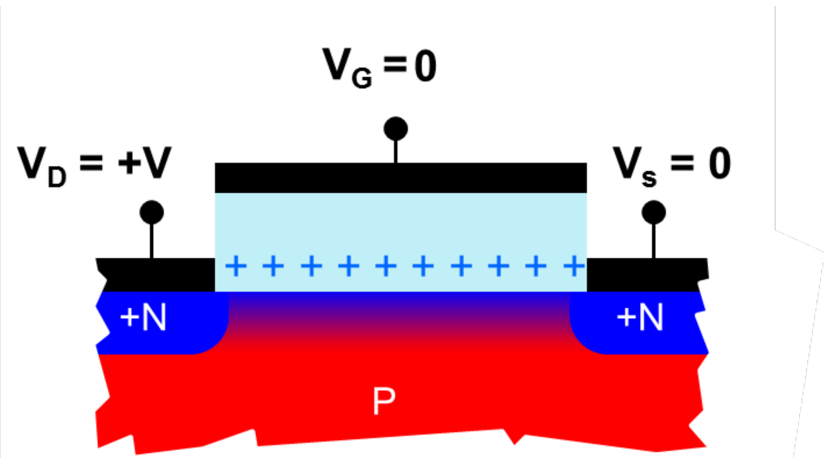
Positive gate voltage

T. R. Oldham and F. B. McLean, "Total Ionizing Dose Effects in MOS Oxides and Devices", IEEE Trans. Nucl. Sci, vol. 50(3), June 2003

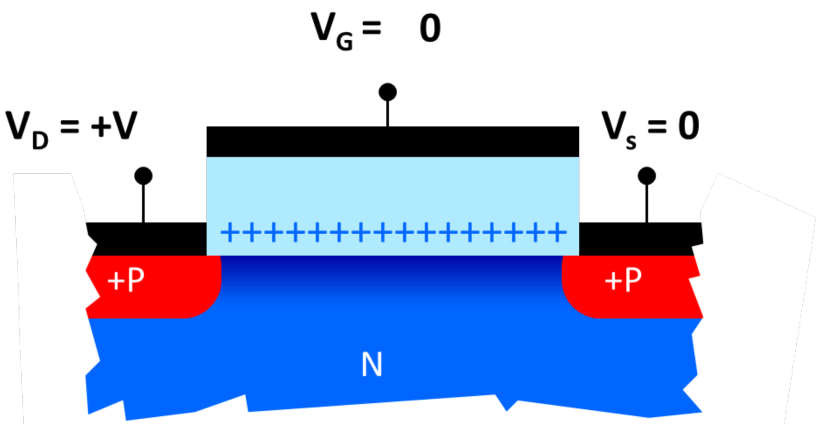


TID depends on radiation type. Photons and electrons are more efficient than heavier ions

TID in MOSFETs



N-channel (NMOS) still "ON" with V_G=0

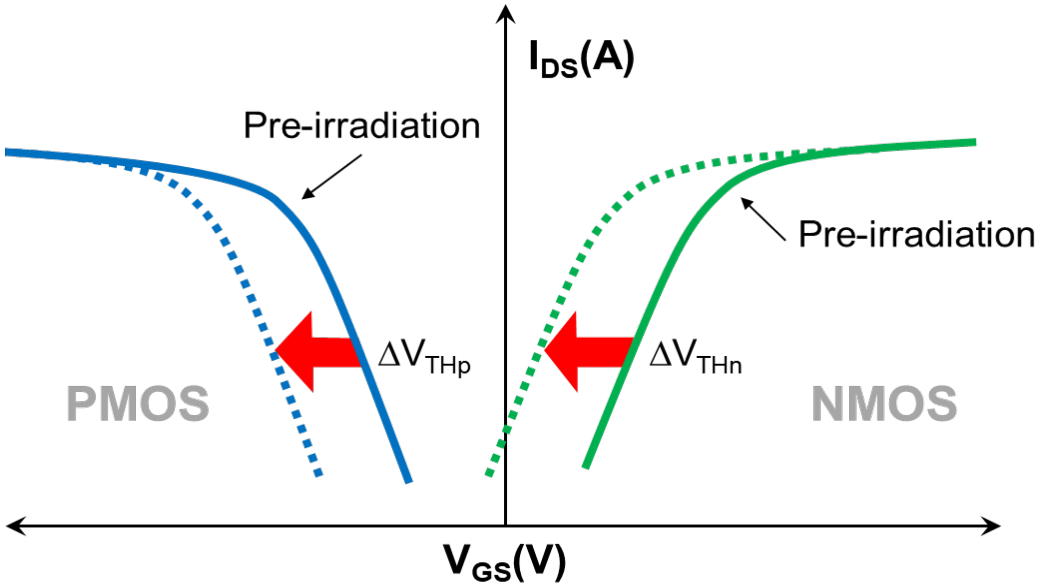


P-channel (PMOS) "OFF" even with V_G=0

POST-IRRADIATION

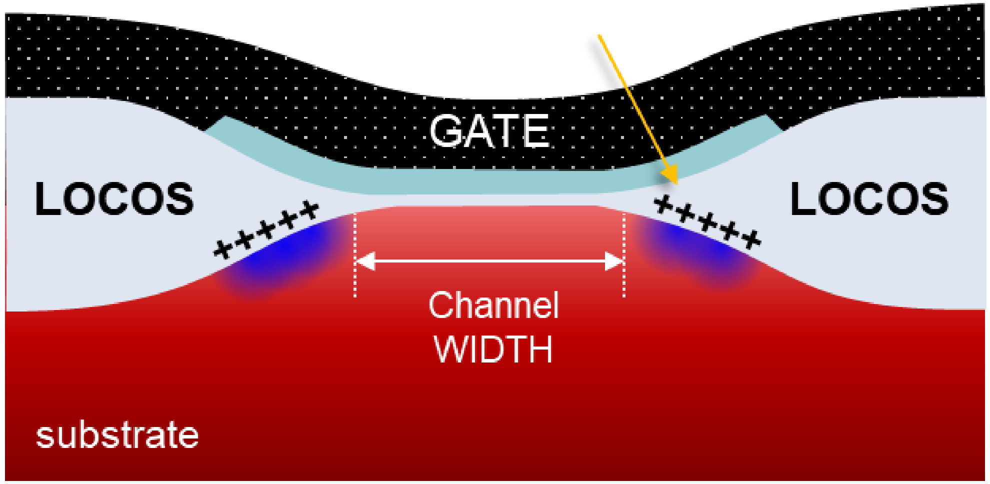
TID + charge creates "leaky faucet“ (harder to turn-off NMOS)

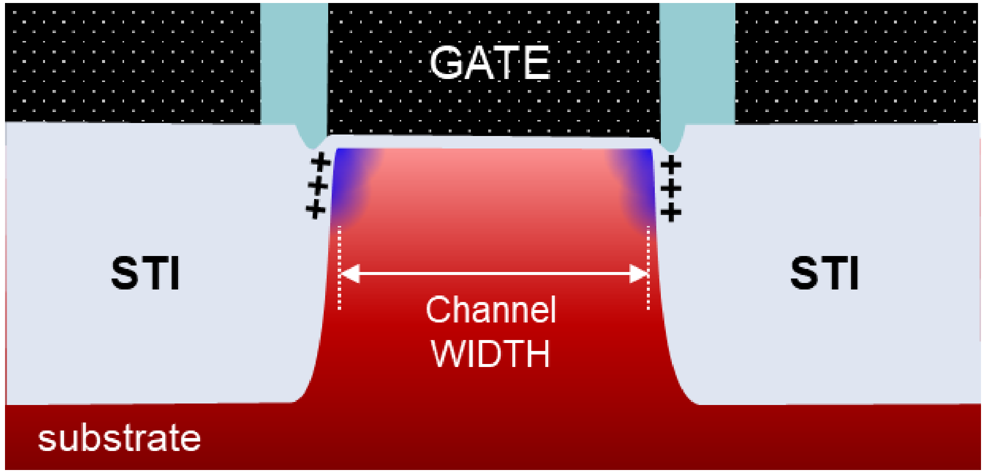
TID + charge creates “rusty faucet“ (harder to turn-on PMOS)



TID induced V_{TH} shift decreases as oxide volume is reduced & channel doping is increased

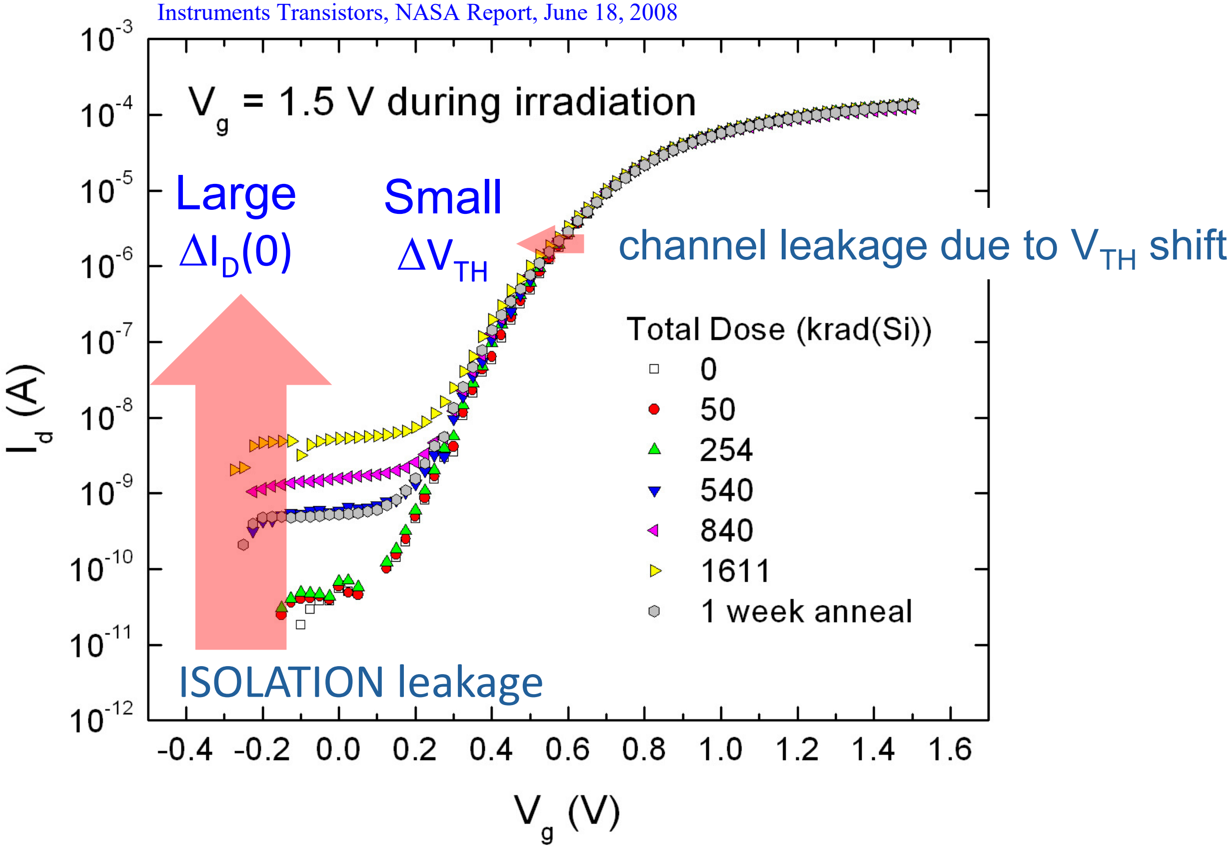
LOCOS & STI Shape Define TID





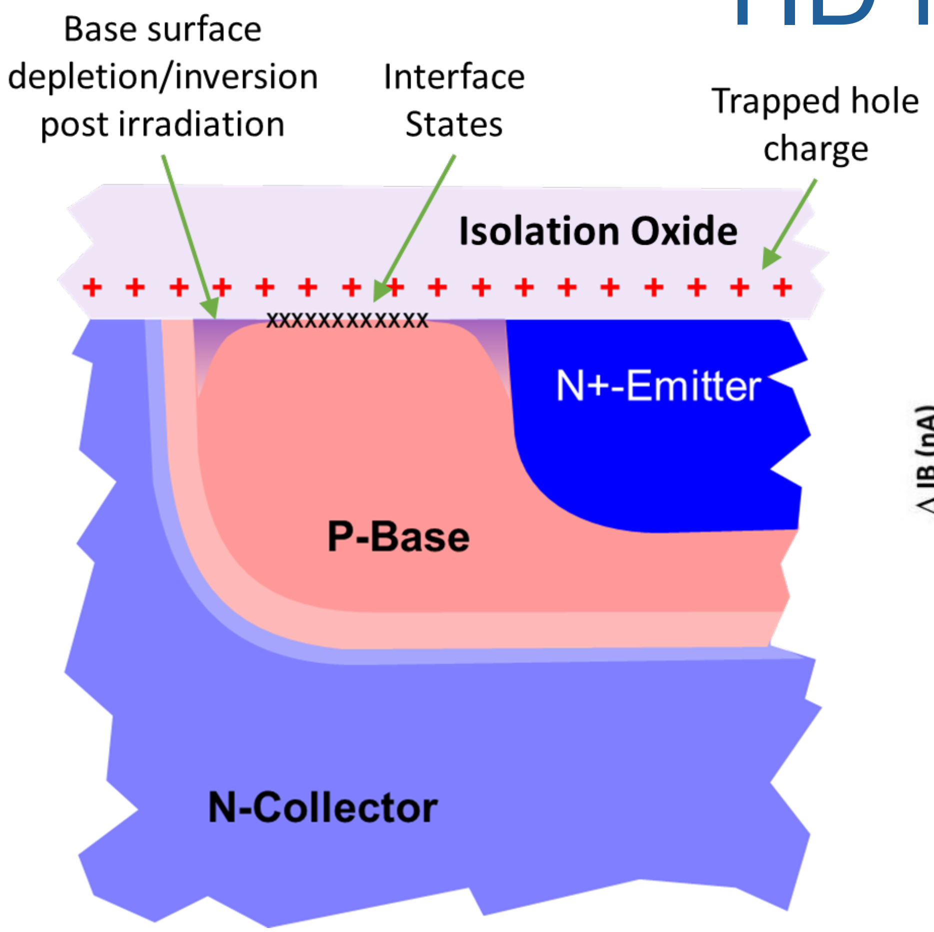
Trapped hole charge (+) in NMOS isolation edges creates parasitic channels that connect source-drain as if transistor were turned on, even when the gate is off.

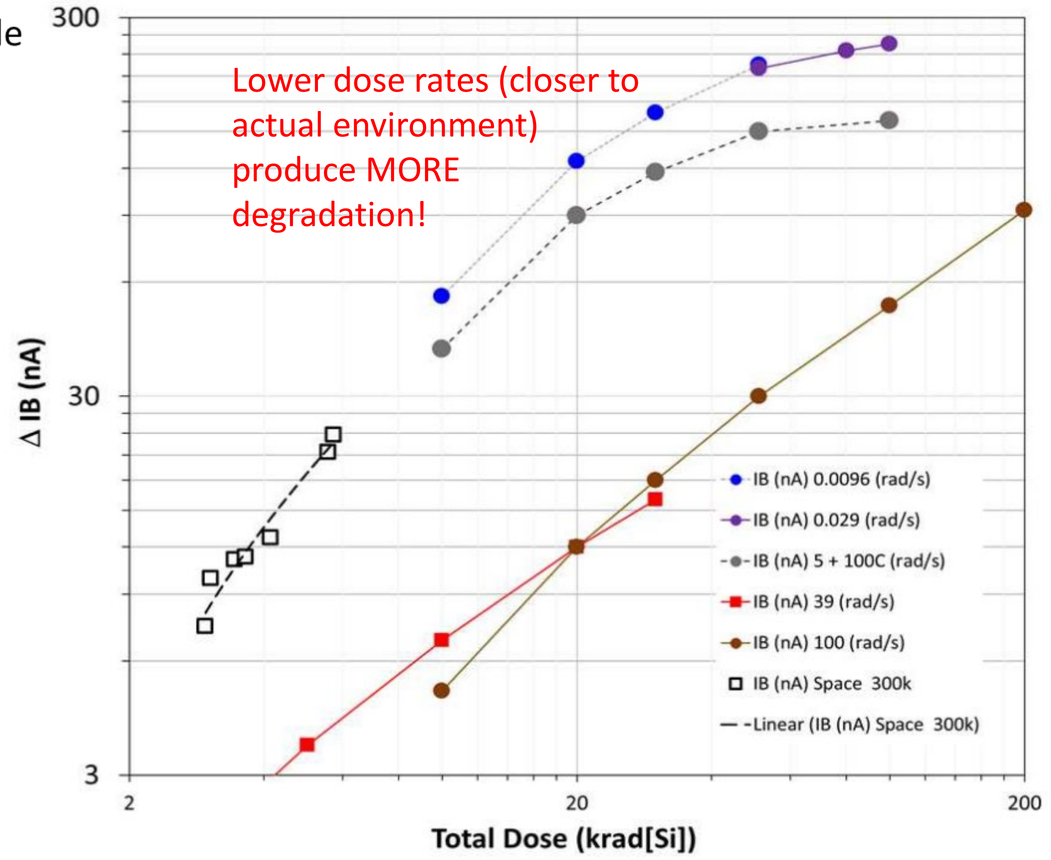
Mike Xapsos, Ken LaBel et al."Total Ionizing Dose Test Results for 130 nm Texas Instruments Transistors, NASA Report, June 18, 2008



Off-state NMOS isolation leakage dominates TID failures in modern CMOS. SOME TID damage can anneal out.

TID in Bipolar Transistors





↑ $I_B \sim R_{bulk(base)} + \uparrow R_{surface(base)}$

Current gain (β) goes down (due to I_B increases) as TID increases

↓ $\beta = \frac{I_C}{\uparrow I_B}$

Single Event Effects (SEEs)

Can only occur in powered circuits!!!

Single event transient

SET →

Single bit upset

SBU

Multiple bit upset

MBU

Single event func. interrupt

SEFI

Single event upset

SEU

SEE

Soft Error

(NDSEE)

Single event latch-up

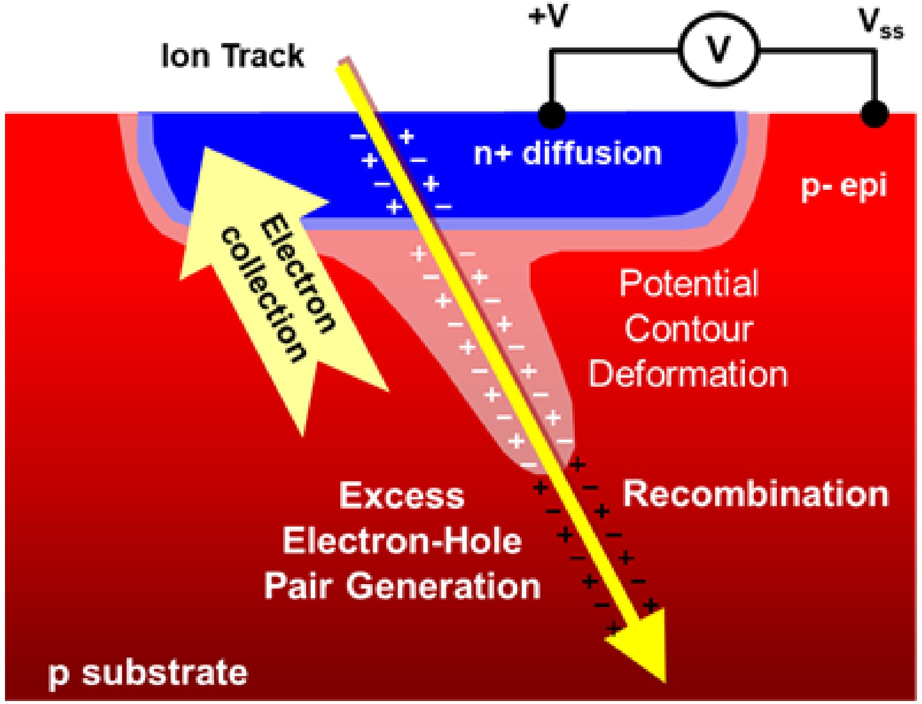
SEL

Single event gate rupture/Burnout

SEGR / SEB

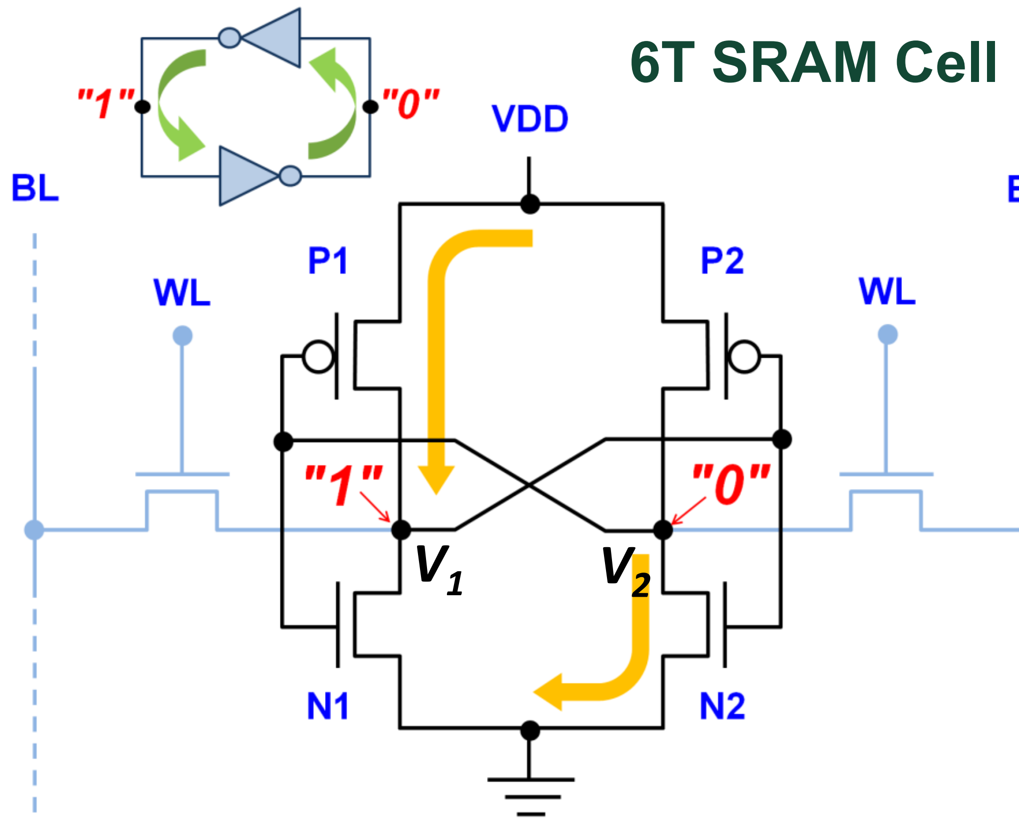
Hard Error

(DSEE)

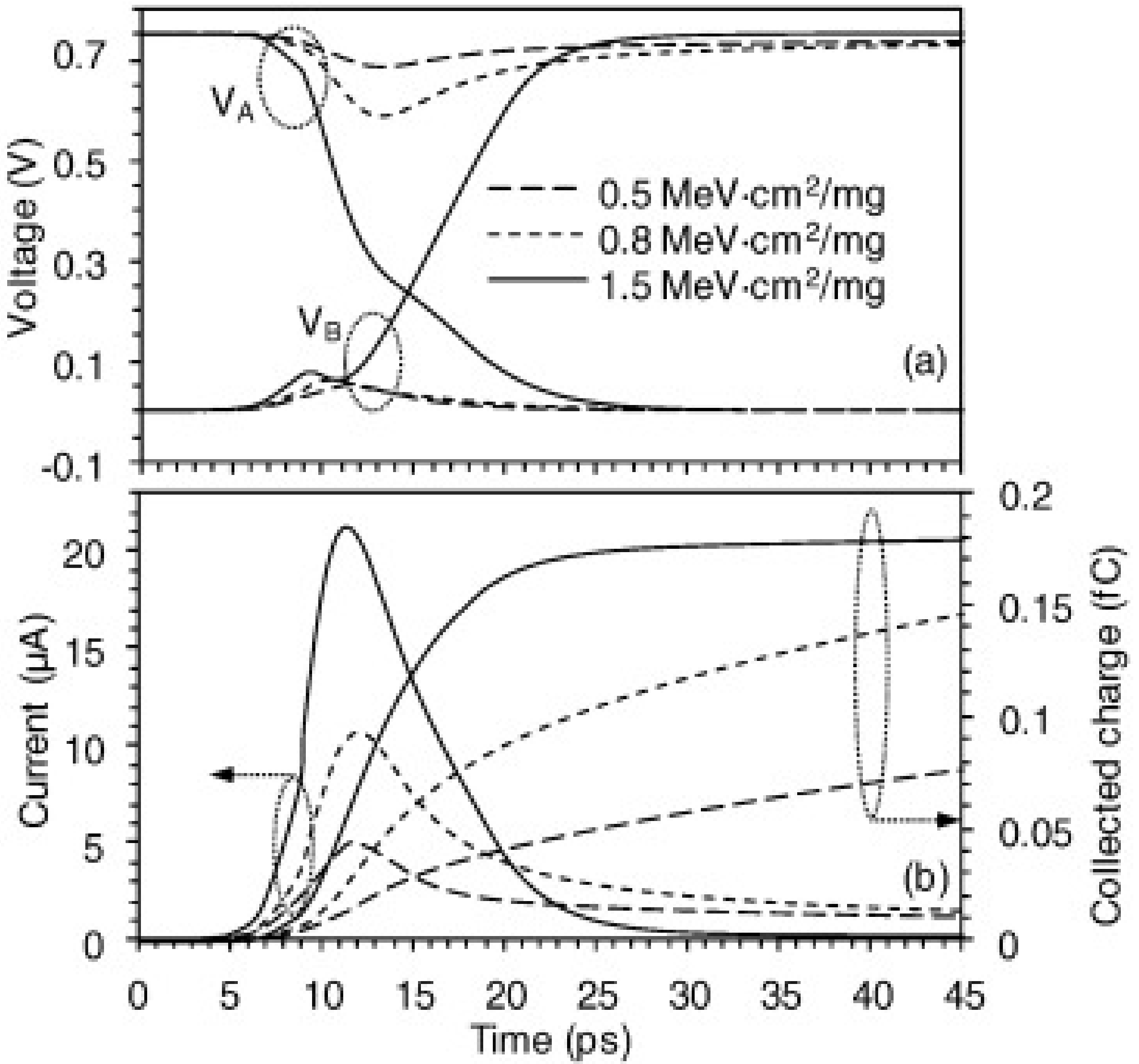


Reverse-biased N+/P junction

Single Event Upset (SEU) in SRAM



More details in I. D. Munteanu and J.L.Autran, "SEU sensitivity of Junctionless Single-Gate SOI MOSFETs-based 6T SRAM cells investigated by 3D TCAD simulation", Microelectronics Rel., 55 (9–10), Aug–Sept 2015, pp. 1501-1505



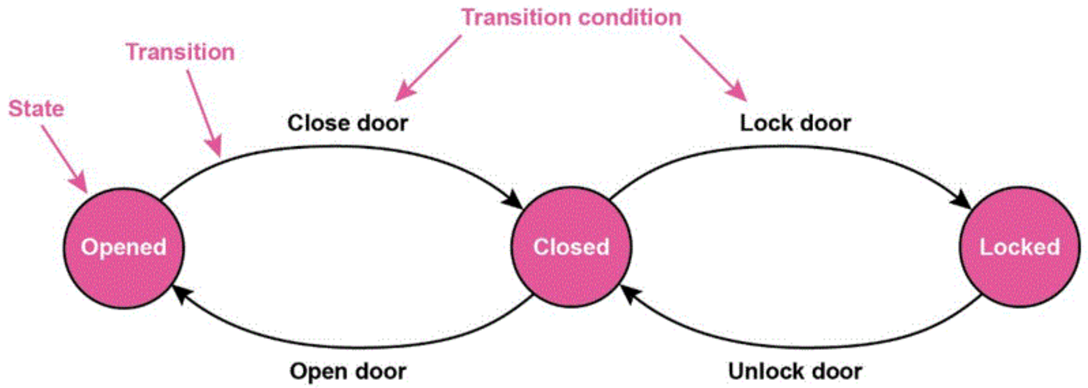
$$Q_{crit} = \frac{1}{2} C_{node} \times V_{node} + I_{restore} \times \tau_{flip}$$

Single Event Functional Interrupt

SEFI occurs when SBU or MBU creates an error in a data-state that CONTROLS the functionality of a state machine (esp. FPGA & processors):

- Reset flop/latch – Event forces system reset
- Address buffer – Event points to wrong address
- Control/Execution to an unknown state (CPU hangs)
- R/W status flop – READ becomes WRITE operation
- Instruction bit flips – Illegal instruction, branching, etc.

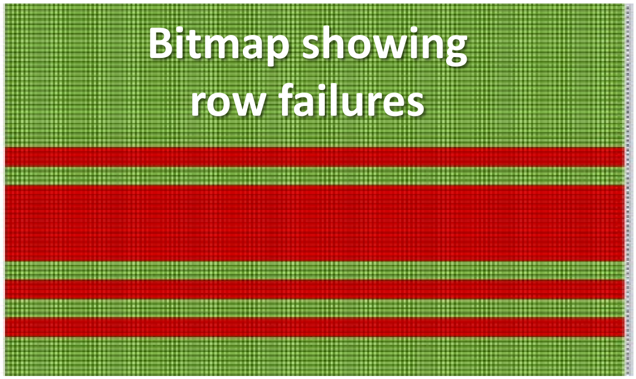
SEFI Modifies the process/function that is being executed – hence its impact can be much greater than SBU or MBU. Processors must be rebooted or re-started to "clear" the SEFI. In some cases, an FPGA (SRAM-based) will need to be reconfigured. Worse case is a processor hang.

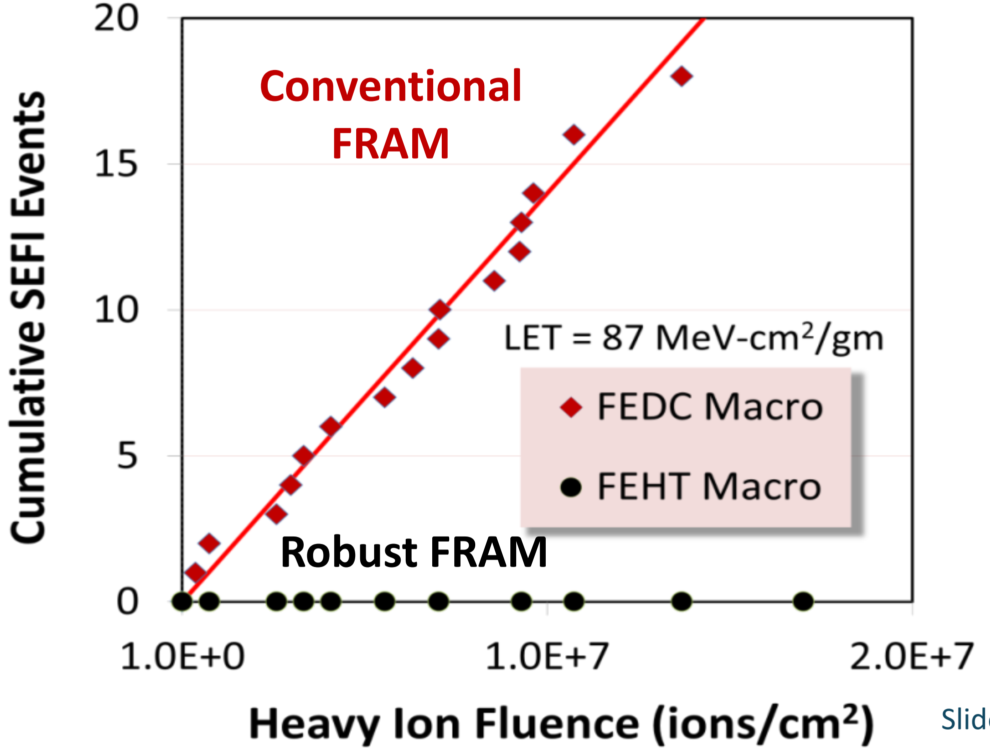


What if SEFI causes "Opened" but "Locked" State?

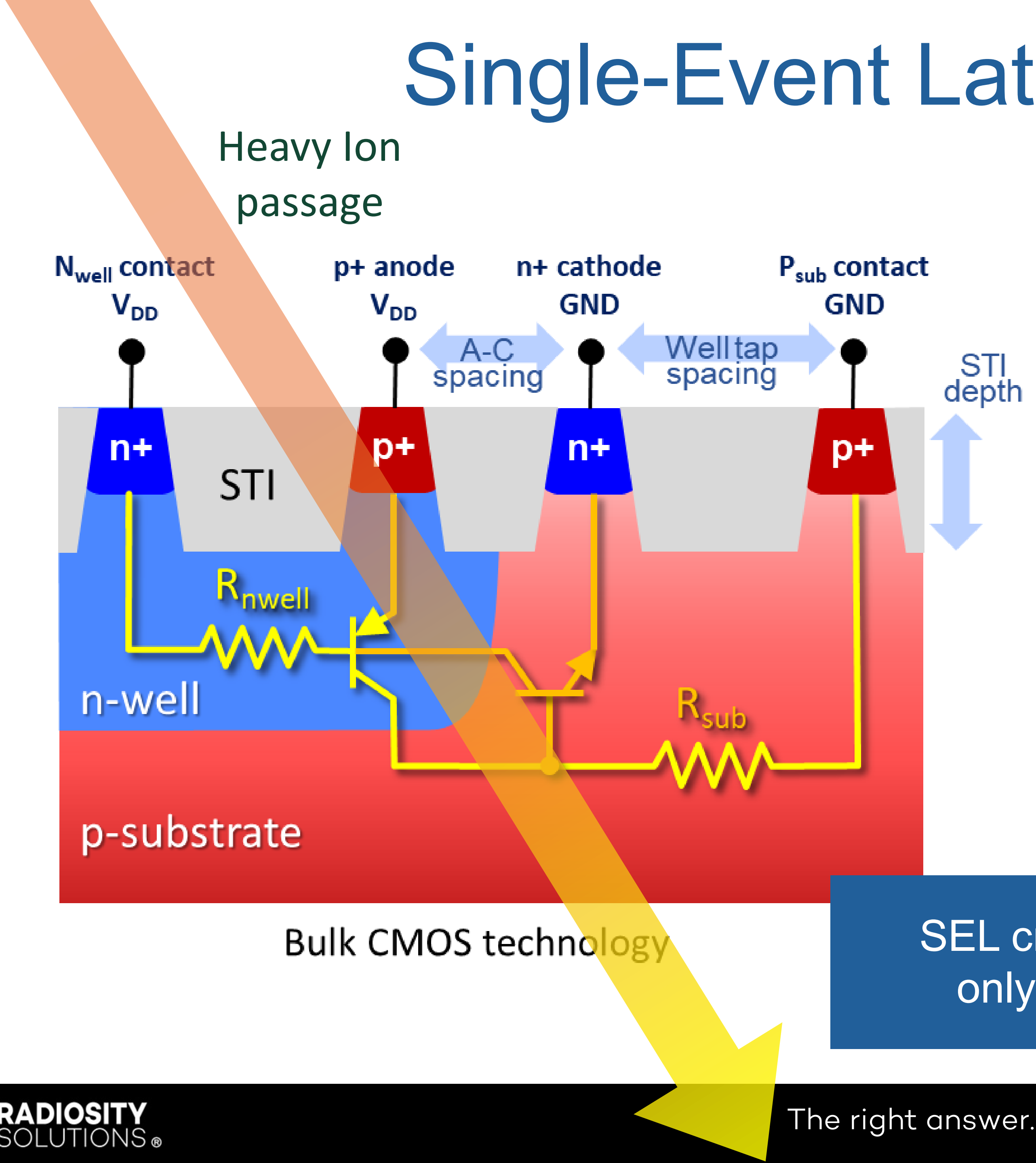
B. A. Dahl et al, "Radiation Evaluation of Ferroelectric Random Access Memory Embedded in 180nm CMOS Technology", 2015 IEEE Radiation Effects Data Workshop (REDW)

Conventional redundancy CMOS SRAM (RSRAM) that translated repair addresses was susceptible to SEU. RSRAM upsets caused SEFIs manifested as block fails of 128-addresses. Once the RSRAM was hardened the SEFI problem was resolved.

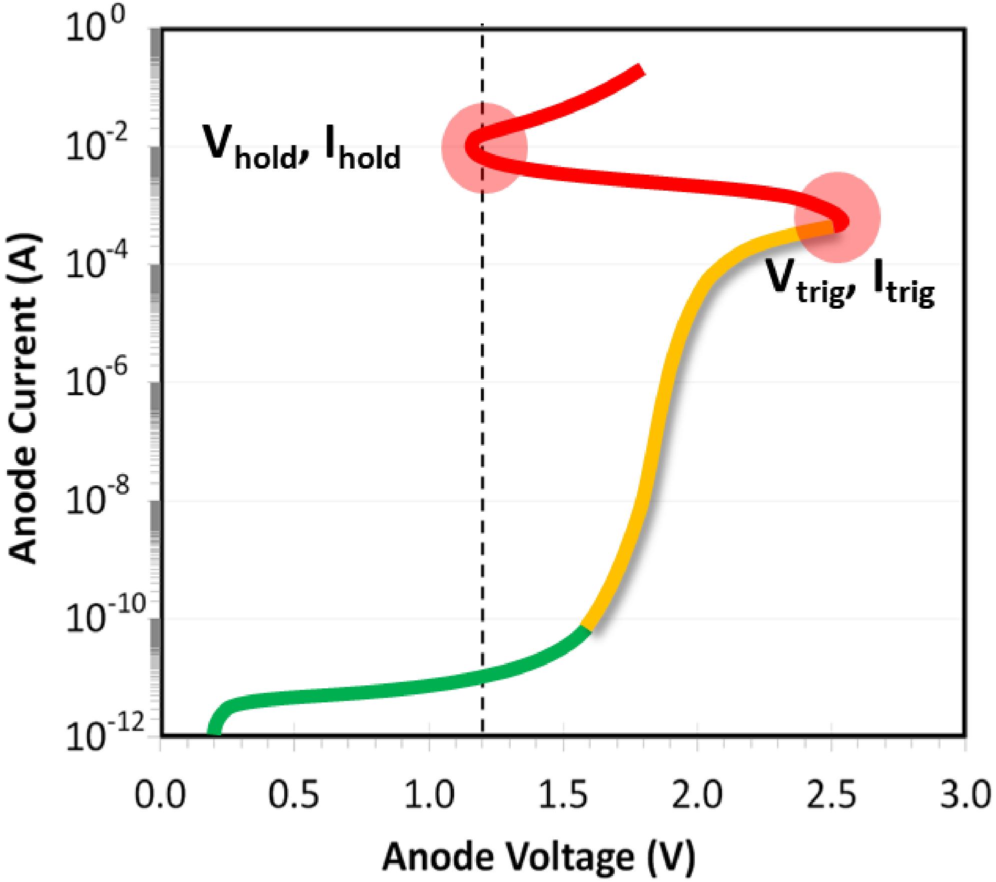




Single-Event Latchup (SEL)



Bulk CMOS technology



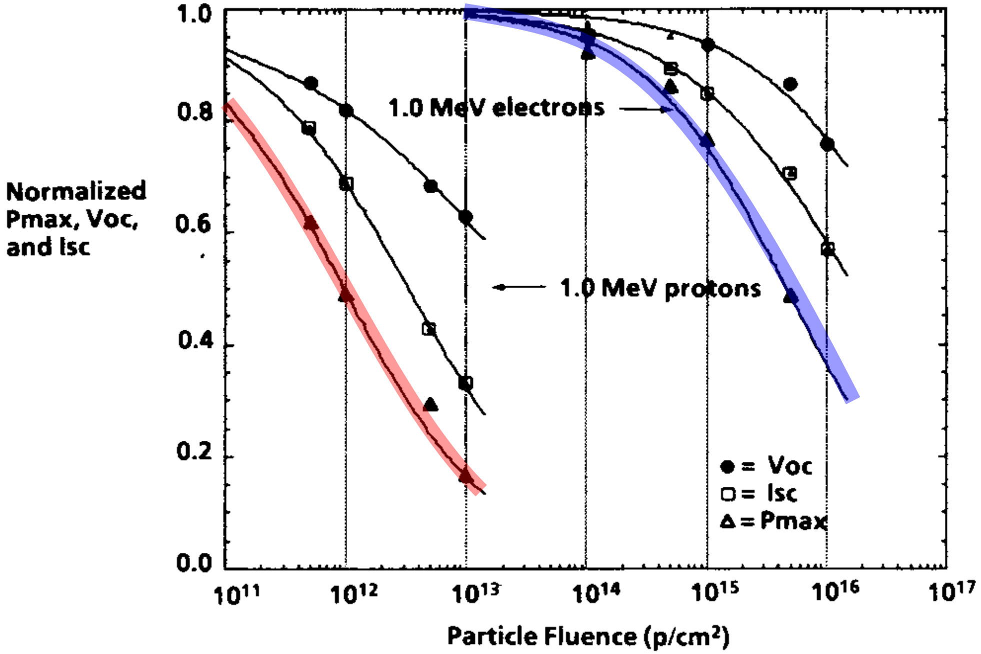
SEL creates a high current "latch" that can only be removed by cycling the power.

Practical Real-World Examples of Radiation Effects

SEL gets worse at higher T so typically reported at 85C to 125C

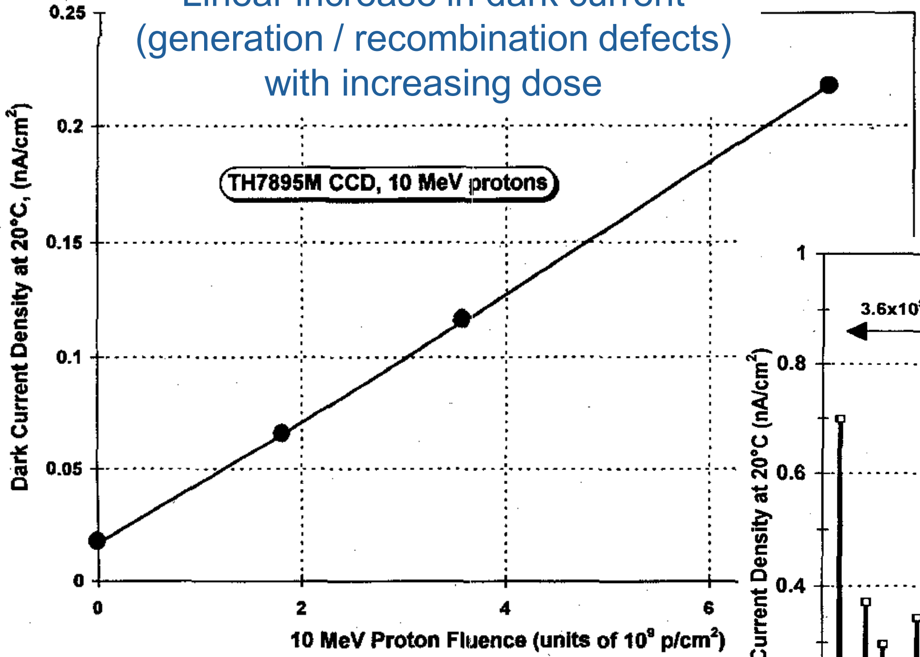
	COTS	**RT** (LEO)	**RH** (GEO)	**SRH** (long deep space missions)	
SEL LET >	1 – 40	30 – 40	40 – 75	75 – 120	MeV-cm^2/mg
TID >	3 – 50	30 – 50	50 – 300	300-1000	krad (Si)
				ITAR Export Control	

"Real World" Impact of DD

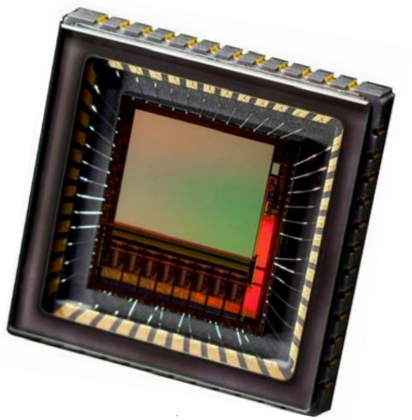


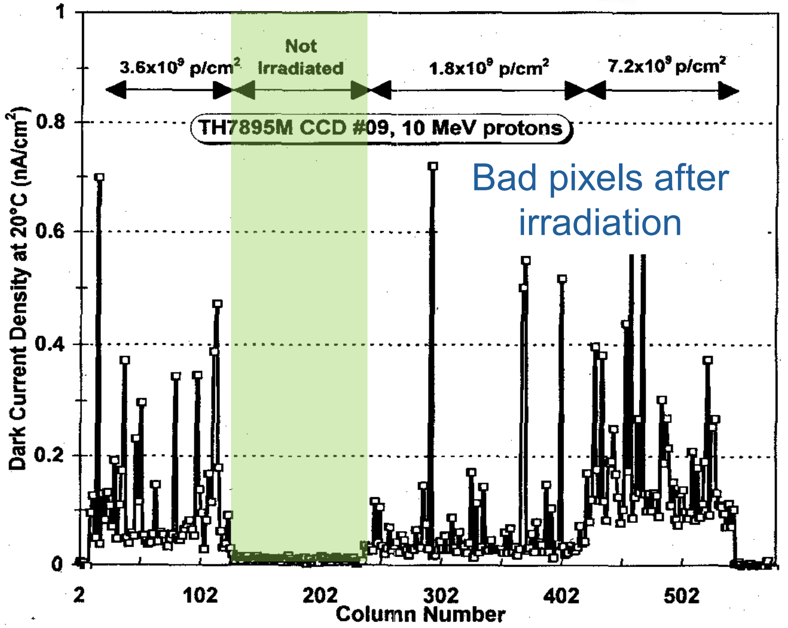
R.M. Burgess et al, "Electron and proton radiation effects on GaAs and CuInSe/sub2/ thin film solar cells," 20th IEEE Photovoltaic Specialists Conference, 1988

Linear increase in dark current (generation / recombination defects) with increasing dose



G. R. Hopkinson, C. J. Dale, and P. W. Marshall, "Proton Effects in Charge-Coupled Devices," IEEE Trans. Nuc. Sci, 43(2), April 1996.



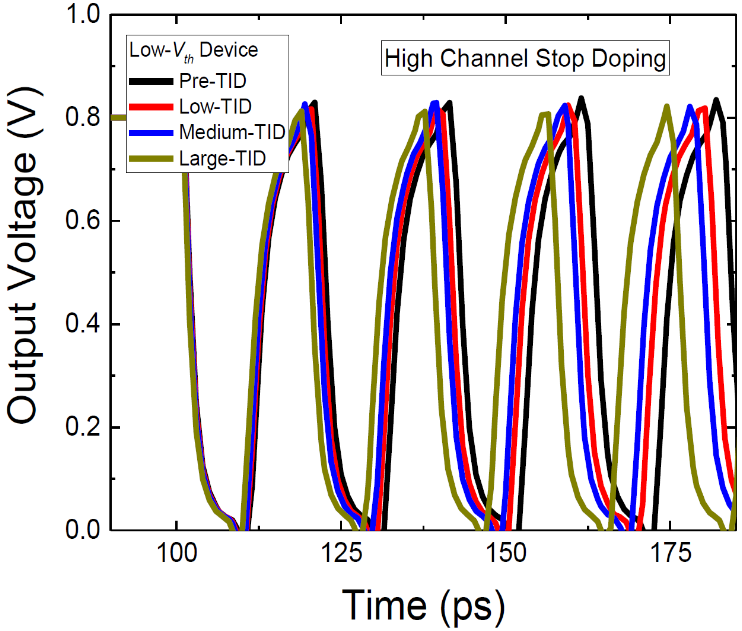


DD reduces solar cell efficiency

DD increases image sensor dark current = lowered dynamic range

"Real World" TID Failures in Digital CMOS

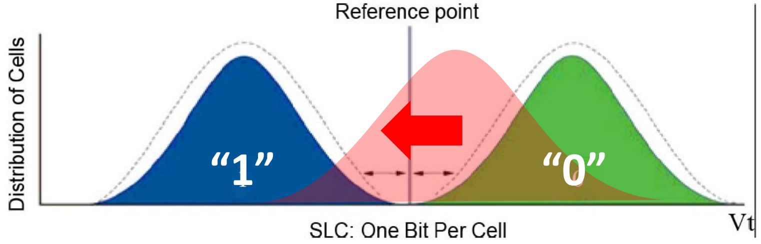
CMOS Ring Oscillators

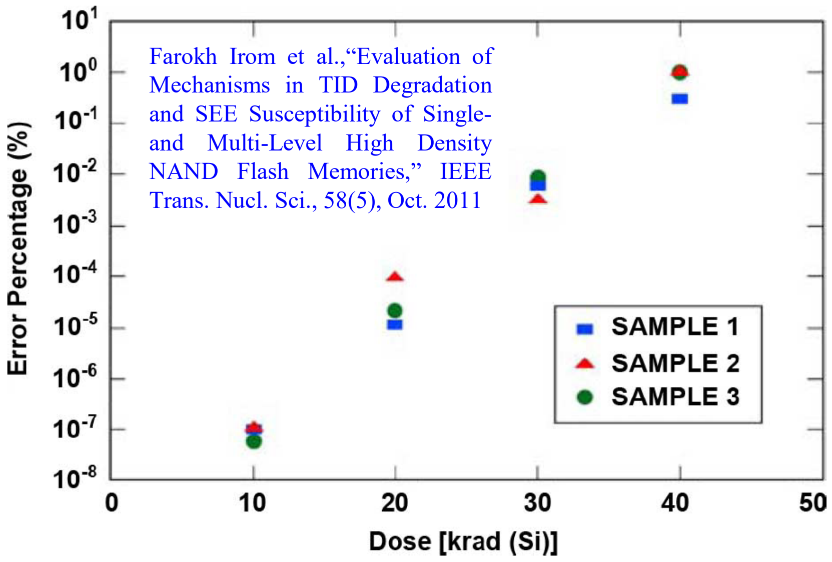


M. P. King, "Analysis of TID Process, Geometry, and Bias Condition Dependence of 14-nm FinFETs and Implications for RF and SRAM Performance," SAND2016-6554J

Timing failures due to V_{TH} shifts lead to critical race or other timing related fails

NAND Flash TID failures



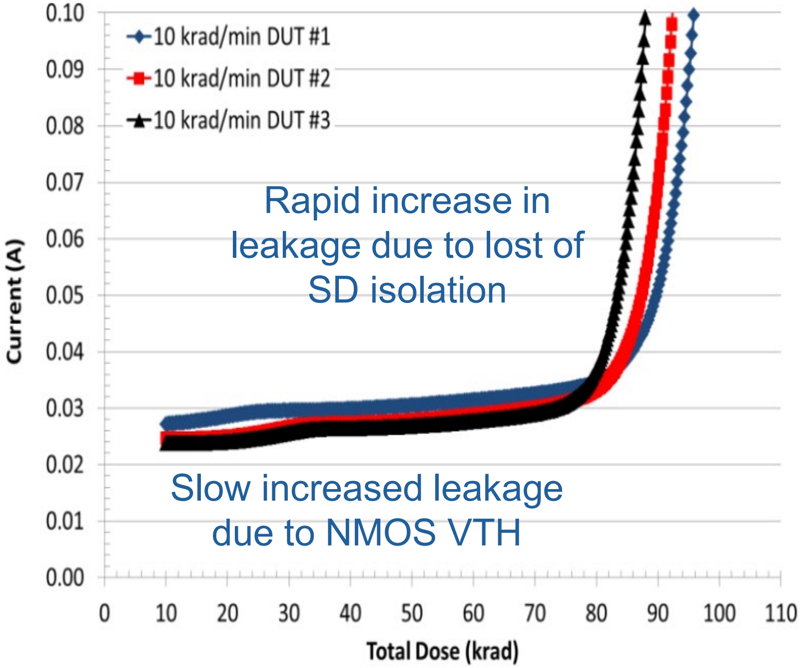


Farokh Irom et al.,"Evaluation of Mechanisms in TID Degradation and SEE Susceptibility of Single- and Multi-Level High Density NAND Flash Memories," IEEE Trans. Nucl. Sci., 58(5), Oct. 2011

Charge pump in FLASH fails (cannot W or Erase)

Digital devices fail due to isolation leakage in NMOS

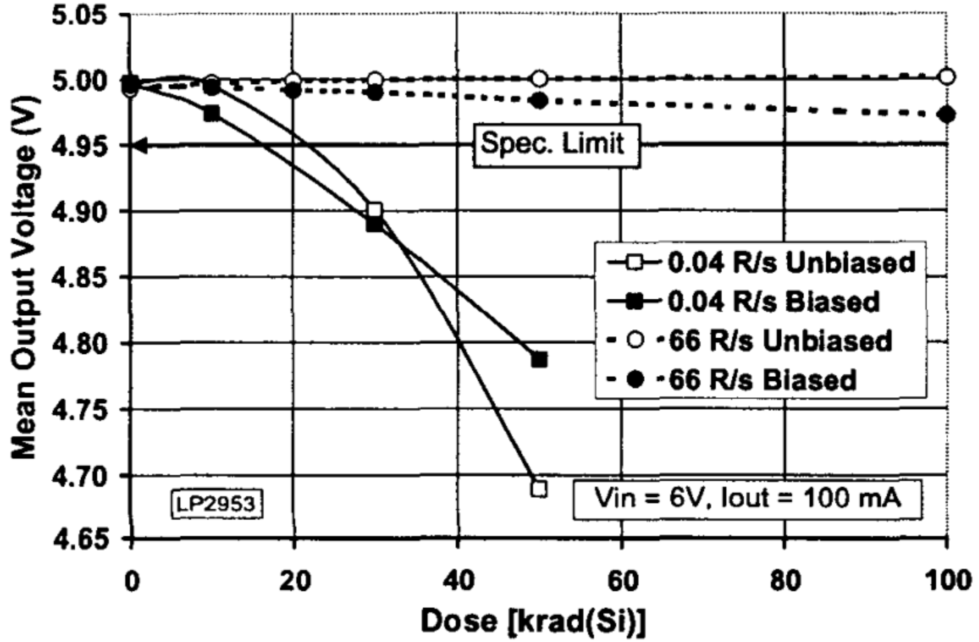
CMOS Current Increase



Nadia Rezzak et al, "Total Ionizing Dose Characterization of 65 nm Flash Based FPGA," IEEE Trans. Nucl. Sci., 2014.

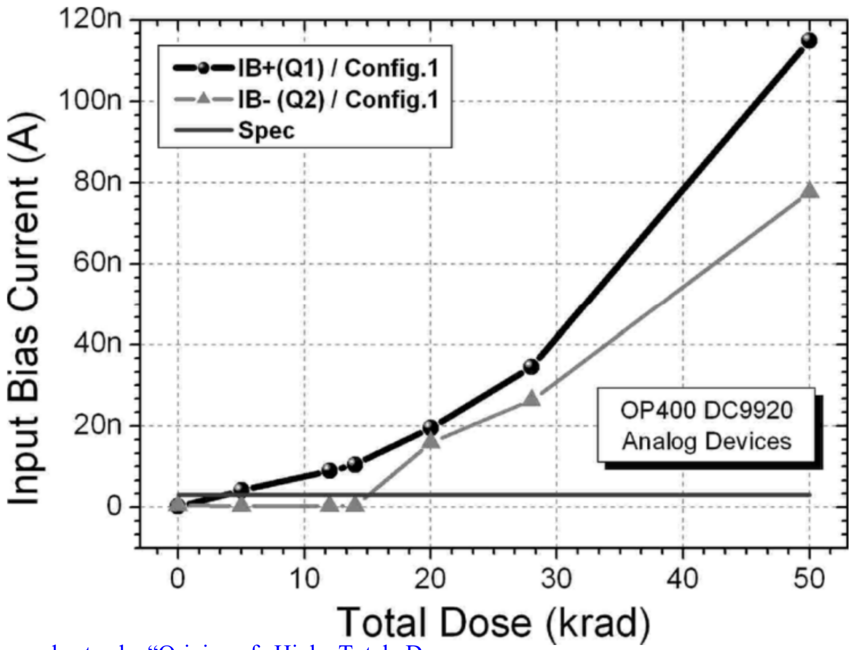
"Real World" TID Fails in BJT-based Analog

LP2953 LDO Regulator



Steven S. McClure et al, "Dose Rate and Bias Dependency of Total Dose Sensitivity of Low Dropout Voltage Regulators", 2000 IEEE Radiation Effects Data Workshop Record.

OP470 Op Amp

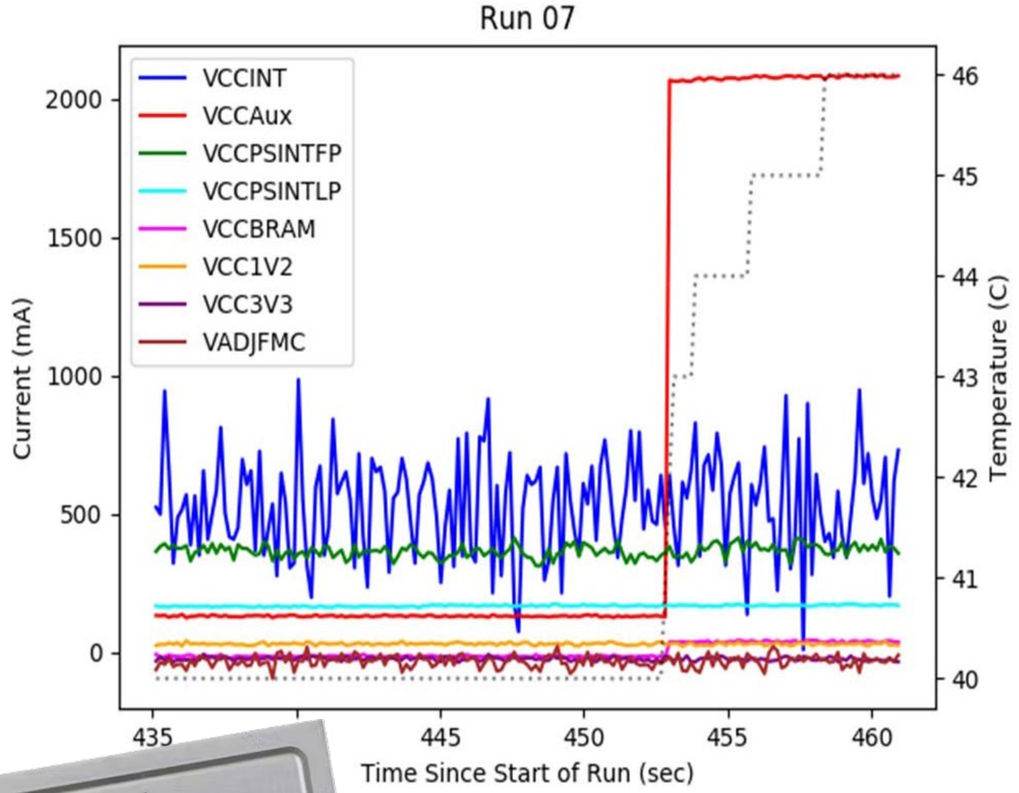


Muriel F. Bernard et al, "Origin of High Total Dose Sensitivity on the OP400 Bipolar Operational Amplifier", IEEE Trans. Nucl. Sci, 55 (6), Dec. 2008

Voltage regulator fails due to loss of voltage and current regulation – note strong ELDRS

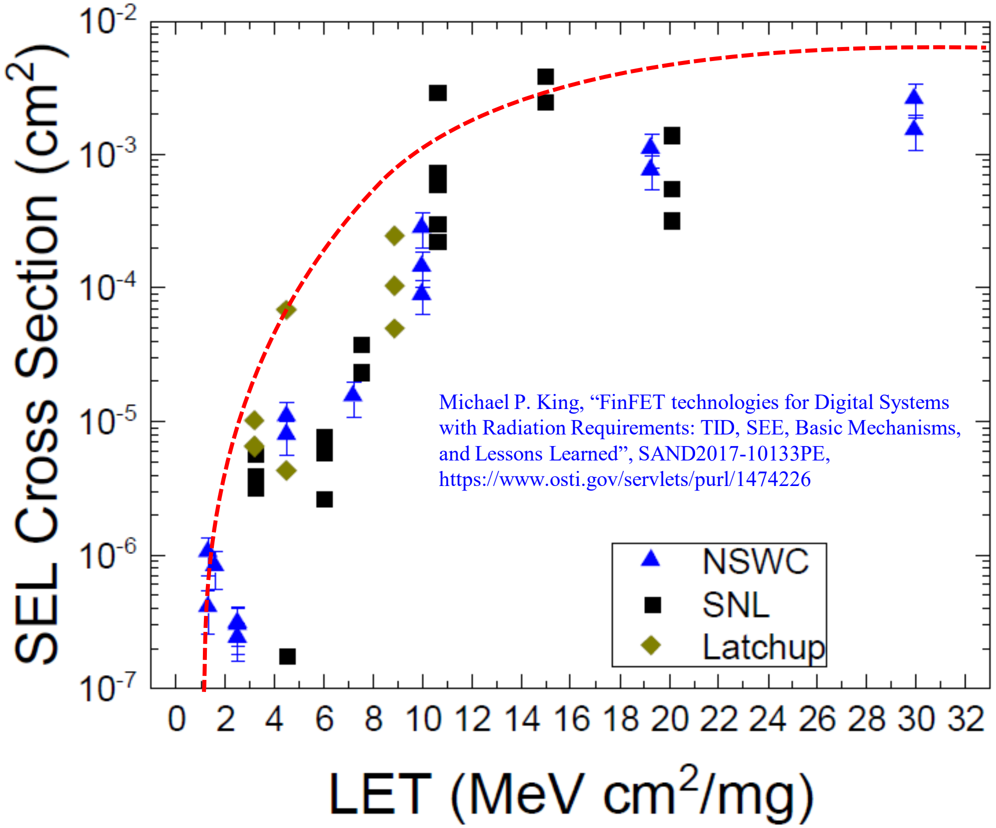
Op amp fails due to input bias increase – this one fails at TID < 5krad!

"Real World" **SEL** Example



R. Koga et al, "Heavy Ion and Proton Induced Single Event Effects on Xilinx Zynq UltraScale+ Field Programmable Gate Array (FPGA)," IEEE Trans. Nucl. Sci, 2018.

David S. Lee et al, "Single-Event Characterization of 16 nm FinFET Xilinx UltraScale+ Devices with Heavy Ion and Neutron Irradiation," IEEE Trans. Nucl. Sci, 2018.



Michael P. King, "FinFET technologies for Digital Systems with Radiation Requirements: TID, SEE, Basic Mechanisms, and Lessons Learned", SAND2017-10133PE, https://www.osti.gov/servlets/purl/1474226

SEL at low LET disqualifies ZYNC FPGA for space! We want SEL-free OR at least no SEL below LET = 40

NASA Guidance on Rasberry Pi Systems

"TID risk is the greatest for Raspberry Pi NAND flash

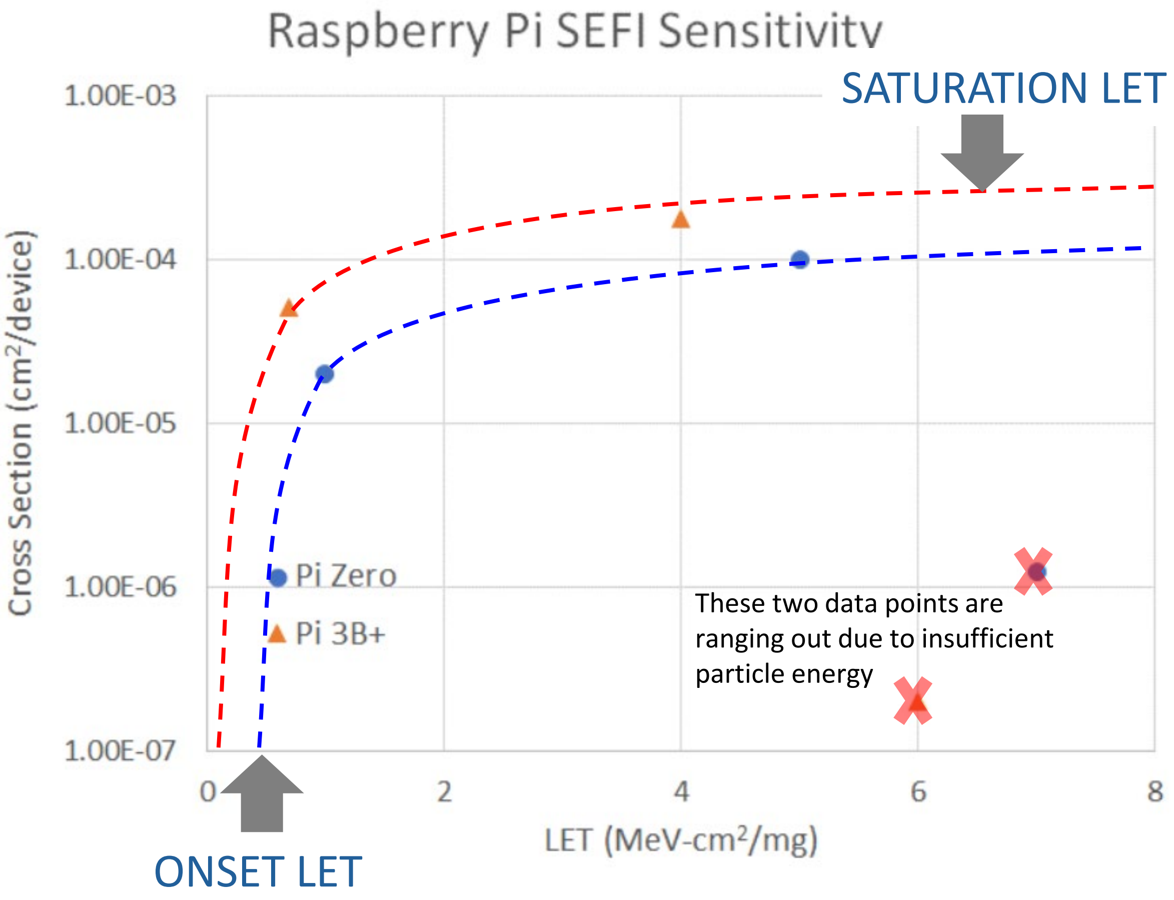
With the high likelihood that the user will be unwilling to refresh the boot image, combined with the potential for outright failure, are likely to create the most significant limitation to use."

But there is good news. There are a huge number of available SD card sizes and manufacturers. In practice, the older "single level cell", or SLC NAND technology tends to perform best for radiation effects.

SD Card TID Failure…most likely caused by a charge pump failure. This may immediately result in never being able to read boot or other data from the SD card. It may also manifest as a system that can partially or completely boot but has general failures any time the Raspberry Pi tries to write to the SD card.

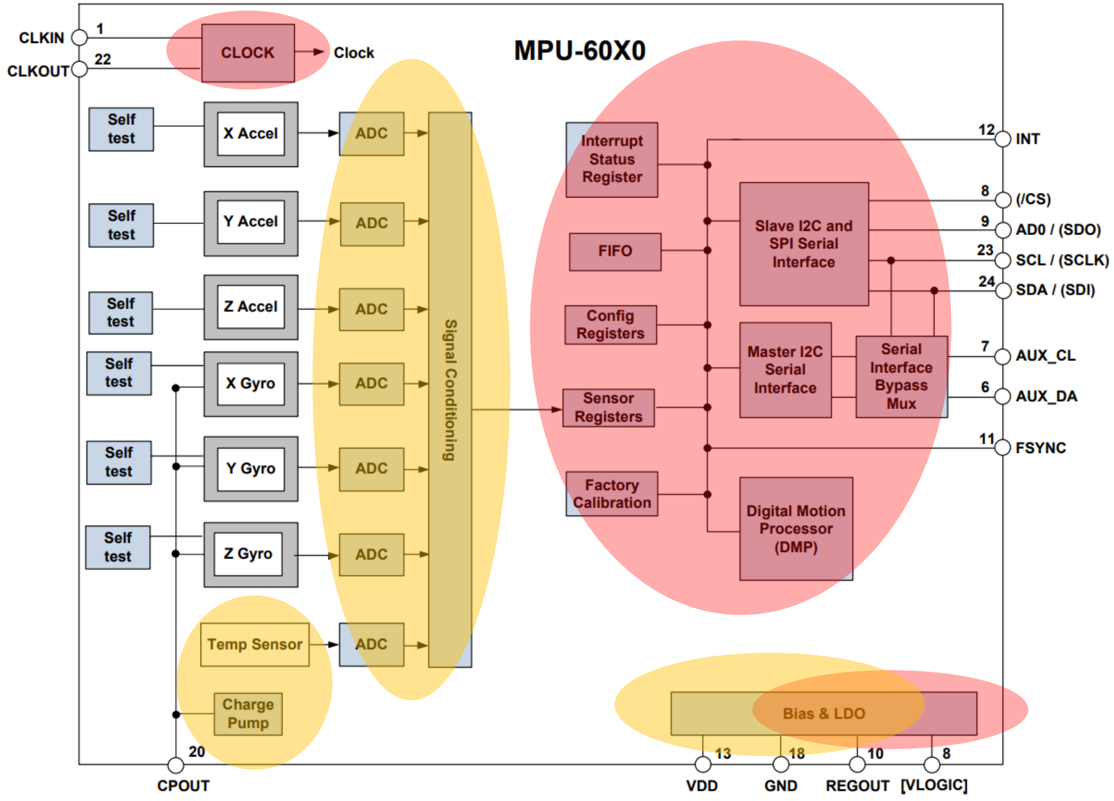
"**Raspberry PIs high operating current**…it was observed that some Raspberry PIs may Increase…system-level current consumption by 2-3x between 10 and 30 krad[Si].

https://nepp.nasa.gov/docs/papers/2021-Guertin-Raspberry-Pi-Guideline-CL-21-5641.pdf



This SEFI result says that you may get on the order of 1 SEFI upset per day or lower, based on a typical LEO orbit.

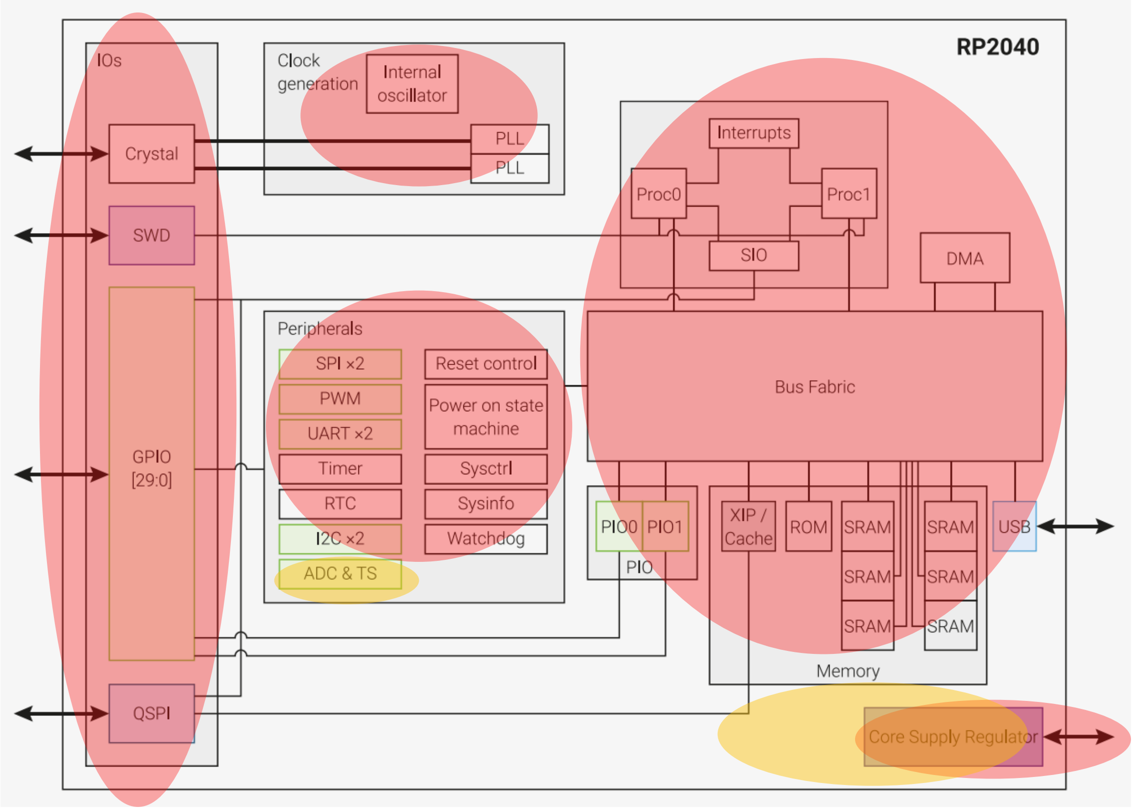
Risk Assessment: ICs from Cubesat BoM



MEM accelerometers will be robust to radiation BUT driving circuits will NOT be.

ADCs and Charge pump will be sensitive to TID. Expect accuracy of Acc. and Gyro channels to get worse over dose. Charge pump maybe compromised – maybe this will kill MEMs if high voltage is used to drive MEMs.

SEE risk in digital interface/compute/clock logic – note ADCs can also suffer from SEE but these will usually be short lived DSETs



Rasberry Pico W (40nm CMOS)

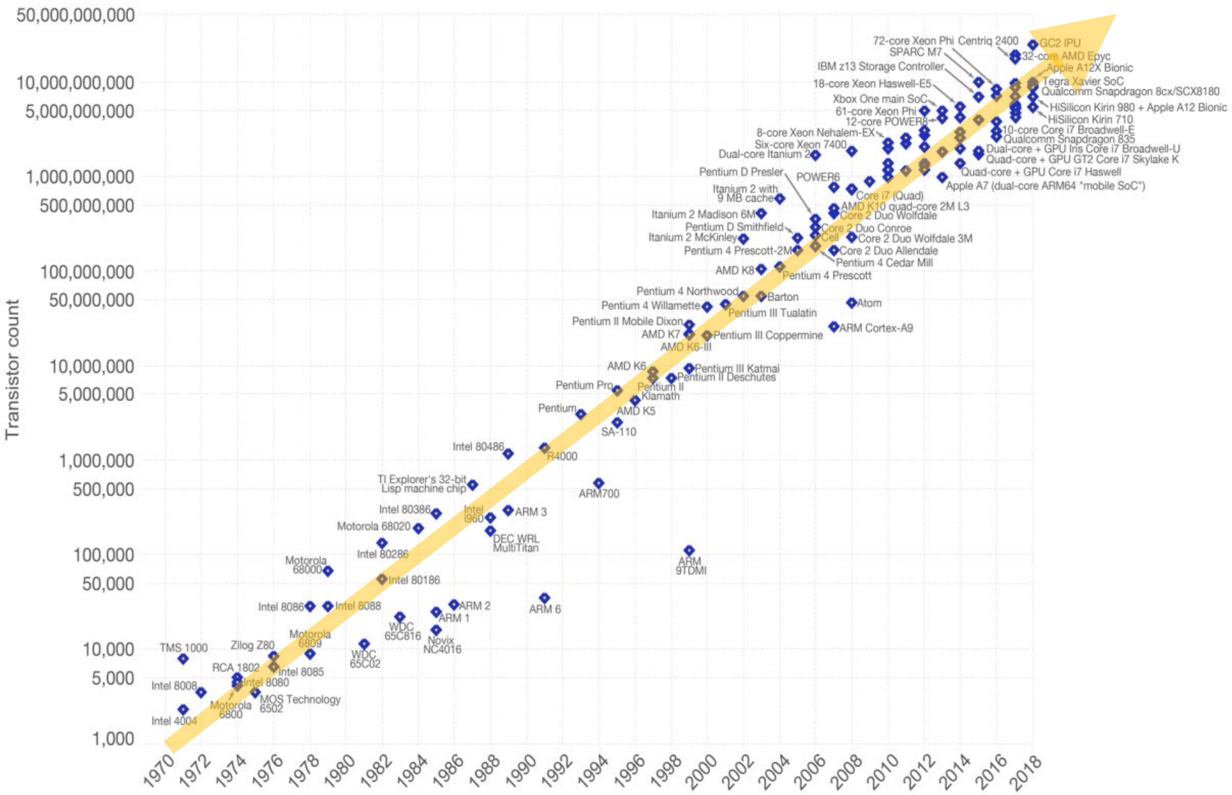
SEE sensitive

TID sensitive

MCU. Mostly a digital device so main fail modes will be SEE. However, power regulator, PLLs, and I/Os may show parametric changes with TID exposure.

General Guidance for Building Space Systems

"New Space" Enablers



By Max Roser https://ourworldindata.org/uploads/2019/05/Transistor-Count-over-time-to-2018.

Density and performance scaling vs. time
~ 10x every 6.5 years

https://www.visualcapitalist.com/the-cost-of-space-flight/

Cost of Orbital Injection
approaching air shipping costs

Key Philosophical Differences

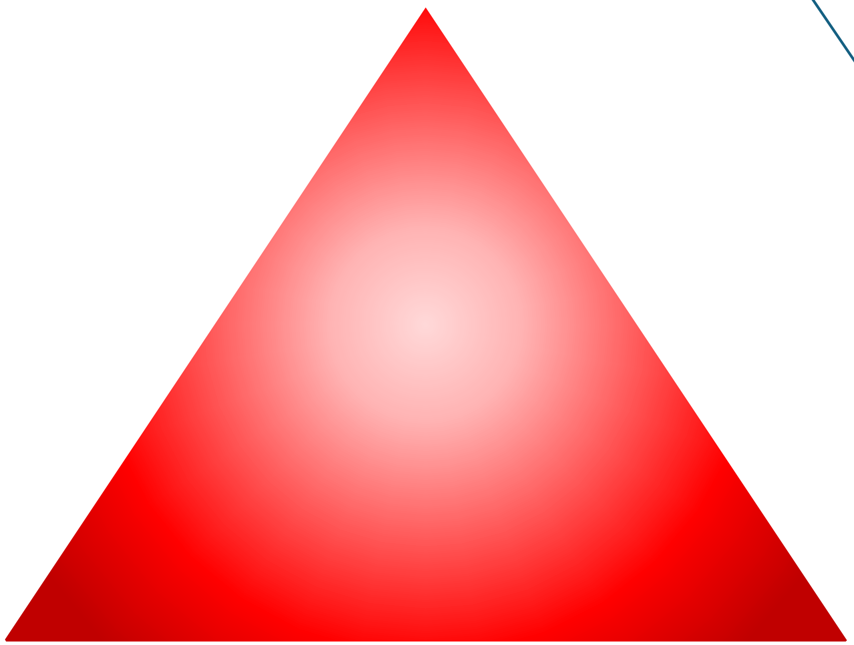
Traditional Space (TS)	***New Space (NS)***
"***Failure is not an option***"	"***Good enough for the mission***"
Large Safety Margins, RDM 2.0 or 3.0	Optimized Margins (just enough?) RDM 1.0-1.5
Long Mission Lifetime (> 5 yrs)	Short Mission Lifetime (< 5 years)
Established procedural heritage	Question all TS procedures
Long Development Windows	Shorter Development Windows
Radhard/Mil-grade/QML	**100% COTS or AEC grade**
Ceramic Pkg.	**Plastic Pkg.**
RLAT, no failures allowed	No RLAT, some failures allowed
Large Budget	**Smaller Budget**

"Perfect is the enemy of good" (enough for the mission) = Limited resources (time, money, info) means you have to focus on a solution for GOOD ENOUGH.

"*Dans ses écrits, un sage Italien dit que le mieux est l'ennemi du bien.*" Voltaire

New Space is about TRADEOFFS!

PERFORMANCE



- Functionality
- Size/weight
- Efficiency (power)
- Functional density
- Reliability
- Quality

SWaP

Reliability / Quality:
- Manufacturing variability
- Test coverage
- B/I, HTOL
- COTS vs. RH/MIL

SCHEDULE

This is the "immovable object" usually tied to a launch date, impact to schedule is most expensive!!!

BUDGET

Don't be "Penny wise, Pound foolish"!!! Cost of test and schedule impact is MUCH more critical than actual component list price.

Primary Reasons For Cubesat Failures?

- Possible reasons for DOA
  - **Compressed development schedule leads to uncaught mistakes** (software errors, mechanisms binding, inadequate power budget, non-robust startup sequences)
  - Shock loads expose workmanship flaws (few hobbyists test for shock)
  - Underpowered RF system
  - Two or more recoverable errors “team up”
  - SEEs
- Sources of early failure
  - Environmental wear (thermal cycling, radiation effects)
  - Low margins (battery depth-of-discharge)
  - Long-term software instability

M. Swartwout, “CubeSat Mission Success: Are We Getting Better?”, CubeSat Developers’ Workshop, 23 April 2019

> “Biggest Threats to CubeSats Missions = Not trading mission scope against fixed schedule and cost”

Common Characteristics of Success

"Process, Process, Process"

Ad-hoc approach spells disaster! **Plan for success**!

"Those that survive the first 90 days tend to stick around"

Implies Quality Marginalities…COTS needs B/I or HTOL?

+ TID

"Plan development schedule w significant functional test and margin"

"You don't know what you don't know" <u>and with COTS there is a lot you don't know</u>

"Bulletproof <u>power-rich safe mode</u> & hard reset from the ground & flight software uploads"

Failure recovery should be given high priority (it's not a question of whether something will fail but WHEN & how does your system respond)

Adapted from M. Swartwout, "CubeSat Mission Success: Are We Getting Better?", CubeSat Developers' Workshop, 23 April 2019

New Space is about the leveraging the TRADES!

- Leverage **“good enough for the mission”…**
- **Define actual radiation environment** as accurately as possible (vs. worst-case).
- Build **radiation & reliability database** early (IEEE, ESA, RADNEXT, NASA, etc.)!
- Eliminate losers early (avoid parts w DSEE, low TID, ELDRS)
- Whenever possible leverage experience - Reuse known good parts. Have plan “B” and “C” READY for test failures (usually RH or RT version of COTS part) before you fail a test!!!!
- Simplify design/BoM to minimize test requirements (rating, type) => use same manufacturer, use small number of values (put in series or parallel). **Each unique component adds risk, test overhead.**
- Work with distributors/vendors to constrain variation (buy lot quantities or ensure same lot purchase). **Spend money on higher reliability grade when called for.**
- **TEST EARLY and OFTEN!** Sample, sample, sample! A lot of radiation testing expense is travel and preparations, maximize utility of the resource for rapid and/or parallel test. Spend time on optimizing test system for throughput.
- **“Feed the Bayesian”** (see papers by Ray Ladbury!!!) – do research and use every source available.

Maximizing chances for mission success!

Shielding has diminishing returns (increasing thickness does less and less) and adds mass (hurting SWaP trade-off). You cannot "shield" your way out of it!

Leverage off the existing literature/databases - Pick mature ICs with existing TID/DD and heavy ion data to minimize weak links (parts with documented weaknesses).

Commercial "NEW Space" usually focuses on COTS parts and tries to screen parts to see if they meet mission requirements (favor established parts over "new and shiny!!!" & consider hardness upgrades):

	COTS	**RT** (LEO)	**RH** (GEO)	**SRH** (long deep space missions)	
SEL LET >	1 – 40	30 – 40	40 – 75	75 – 120	MeV-cm^2/mg
TID >	3 – 50	30 – 50	50 – 300	300-1000	krad (Si)

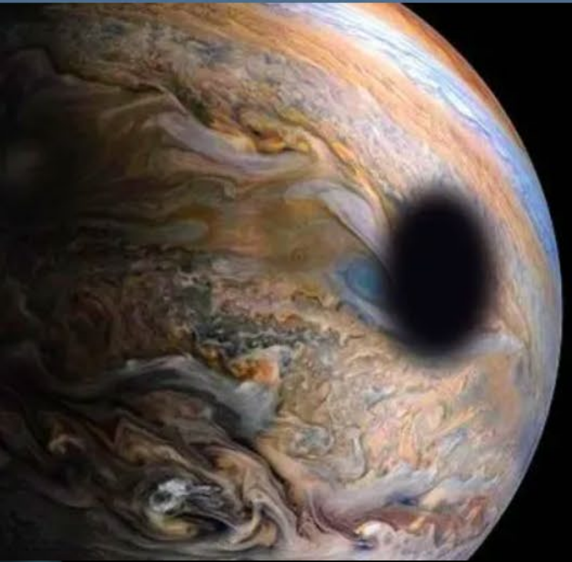
Implement a **remote reset/reboot feature** to recover from device hangs (SEFI) without ground station intervention. Use current monitors/limiters tied to reset circuit for autonomous SEL detection and recovery.

OUR PRINCIPAL CONSULTANT

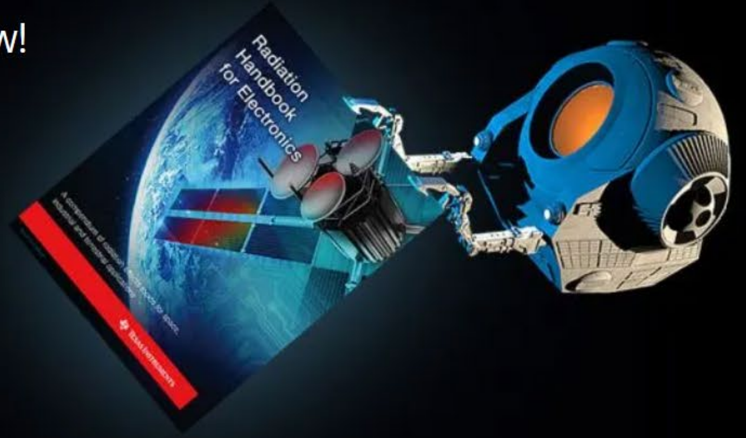
Robert C. Baumann, IEEE Fellow, Ph.D.

- **Internationally recognized expert** in radiation effects in microelectronics.
- **29 years at Texas instruments,** Chief Technologist & TI Fellow (emeritus).
- **Proven track record** of radiation testing, modeling, and numerous process and design radiation hardening successes. Many industry firsts.
- **Standards authority**: Co-authored/led the development of industry-standard JEDEC JESD89 radiation effects test methods.
- **Export Control**: Co-led SIA Expert Panel to shape U.S. ITAR export controls to account for technology advancements.
- **Director of Radiation Effects and Reliability** and IEEE Fellow at Center for Harsh Environment Semiconductors and Systems at U. of Texas at Dallas.
- **Publications**: 100+, 17 patents, several book chapters, and primary author of TI's renowned "Radiation Handbook for Electronics."

MORE BIOGRAPHICS



Start your SPACE ODYSSEY now!



GRAB YOUR HANDBOOK NOW!

https://www.ti.com/applications/industrial/aerospace-defense/space/radiation-handbook-for-electronics.html


ΕΥΧΑΡΙΣΤΩ
TÄNAN
HVALA
GRACIAS
DZIĘKUJĘ
TACK
GRAZIE
ありがとう
MERCI
THANK YOU
DIAKUIU
PALDIES
ACIU
TAK
DANKE
DANK U WEL
ДЗЯКУЮ
СПАСИБО
谢谢
OBRIGADO
diolch
KIITOS
TESEKKUR EDERIM

Total Ionizing Dose
Lab Notes

3 Key Radiation Effects

- **Transient charge generation in semiconductors**
- **Charge trapping in insulators**
- **Displacement damage**

Total Non-Ionizing DOSE
(TNID, DD)

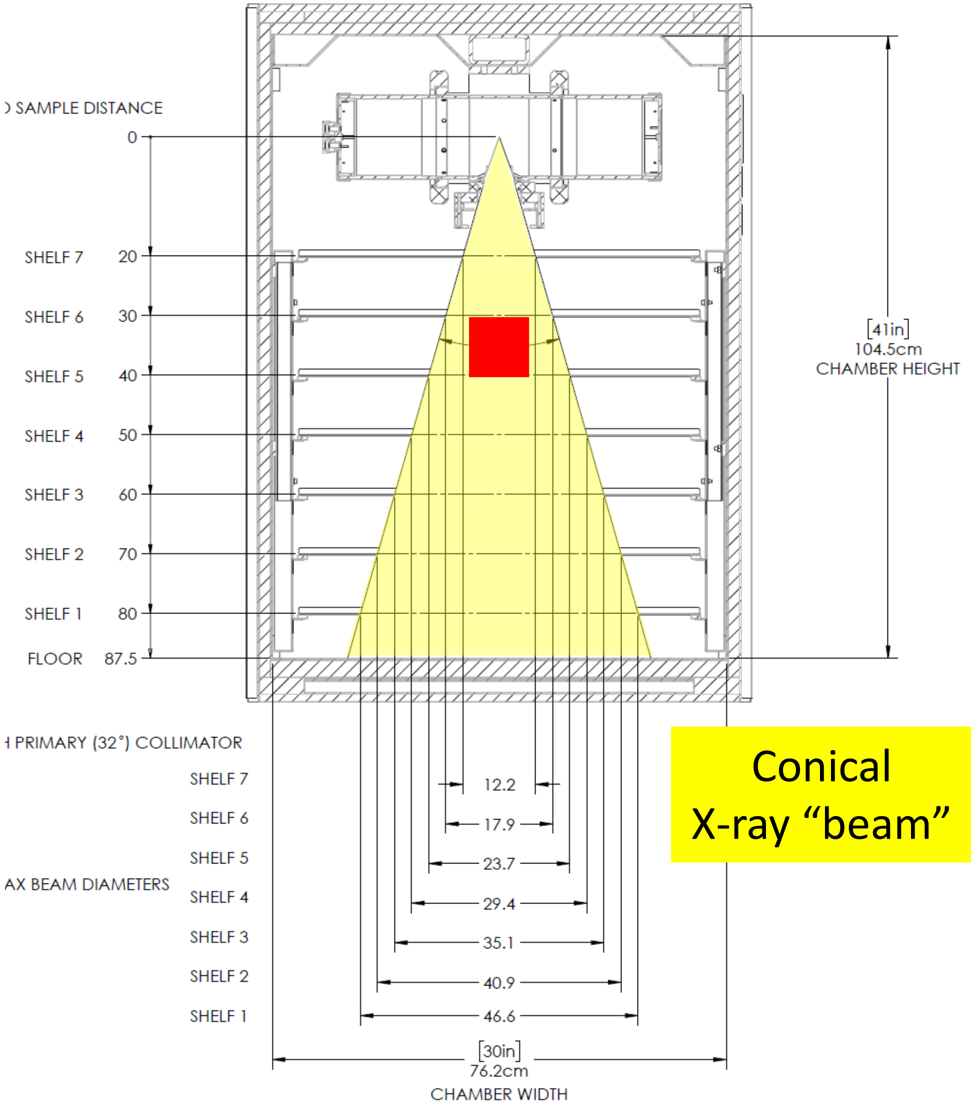
Total Ionizing DOSE
(TID)

Single Event Effects
(SEEs)

Makes NMOS more leaky
Shifts VTH in both PMOS/NMOS
Makes BJTs lower gain (higher base current)

High Voltage X-Ray Irradiator (TID)

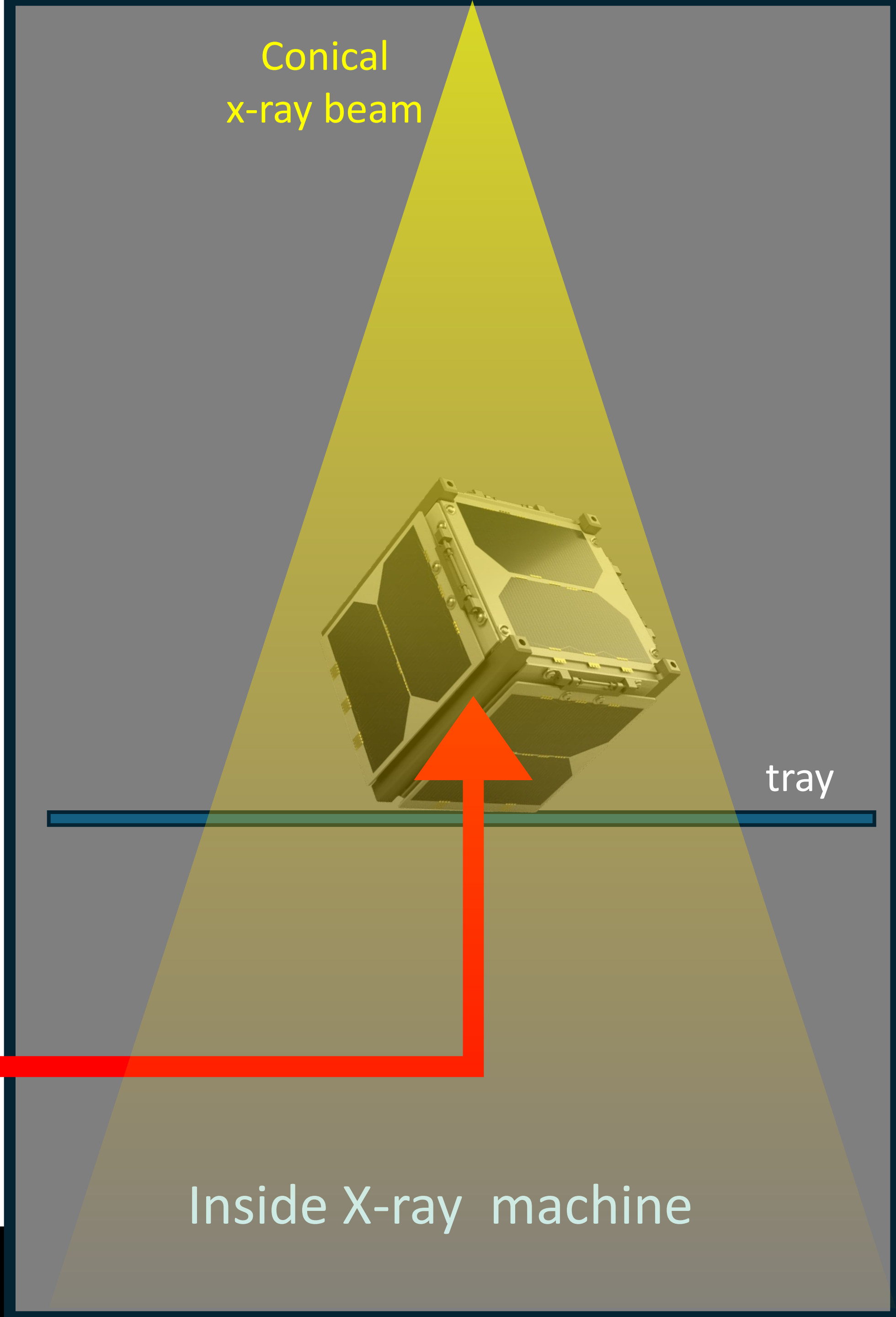
Tube Potential: 320kV / 12.5mA
Filter: Aluminum
Max. Power: 4000 W
Irradiation Area: 23.7 cm diam.



Conical X-ray "beam"

Basic Setup

Hard connection for monitoring cubesat "health" during irradiation. We also have a wi-fi option if hard connection fails due to interface chip failure. We have back up SD cards with OS/boot code so we can irradiate through SD failures.



What are we going to do?

Filter 1

From dosimetric analysis by Dr. Rodolfo Rodriguez-Davila

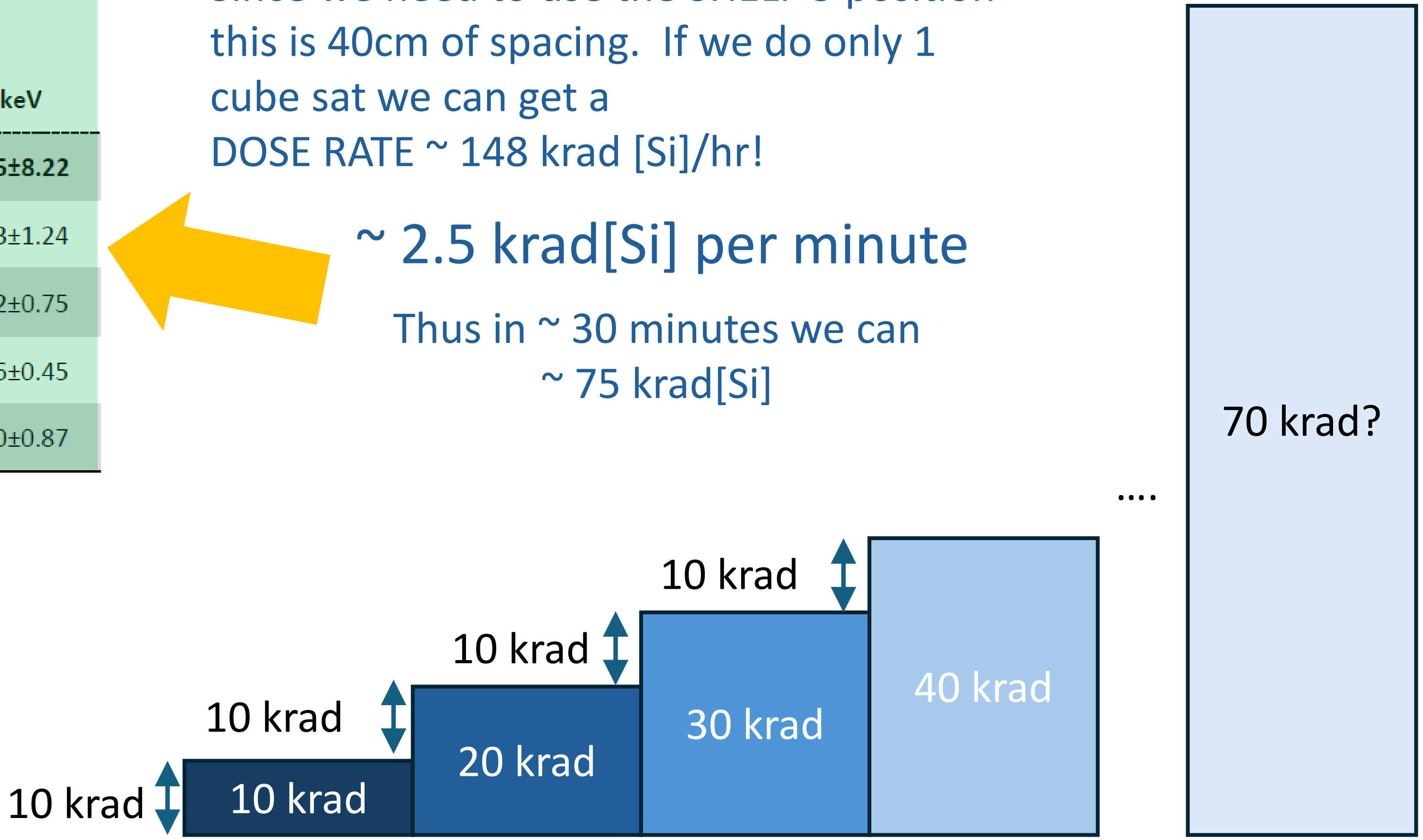
cGy [Si] = rad [Si]	Dose Rate (cGy/min)			
Position	50keV	80keV	160keV	320keV
30	83.00±0.73	208.29±2.13	555.17±5.31	849.35±8.22
40	45.83±0.45	115.49±0.98	304.13±3.01	469.33±1.24
50	28.83±0.05	72.19±0.66	192.66±1.80	297.22±0.75
60	19.55±0.15	48.60±0.46	130.17±1.08	207.86±0.45
80	10.89±0.02	27.54±0.060	73.74±0.17	113.60±0.87

Since we need to use the SHELF 5 position this is 40cm of spacing. If we do only 1 cube sat we can get a DOSE RATE ~ 148 krad [Si]/hr!

~ 2.5 krad[Si] per minute

Thus in ~ 30 minutes we can ~ 75 krad[Si]

Keep stepping up dose until cubesat fails



A word about dose units and conversions:

cGy [H_2O] = Rad [H_2O]

Rad [Si] = 5.294 * Rad [H_2O]

For 10krad[Si] we need to set the machine's target dose to ~ 1889 cGy[H_2O]

We are monitoring various system variables every couple of seconds continuously during the irradiation – we take steps 10 krad[Si] so we can fix any issues like SD cards failing (each step last ~ 4-5 min).